

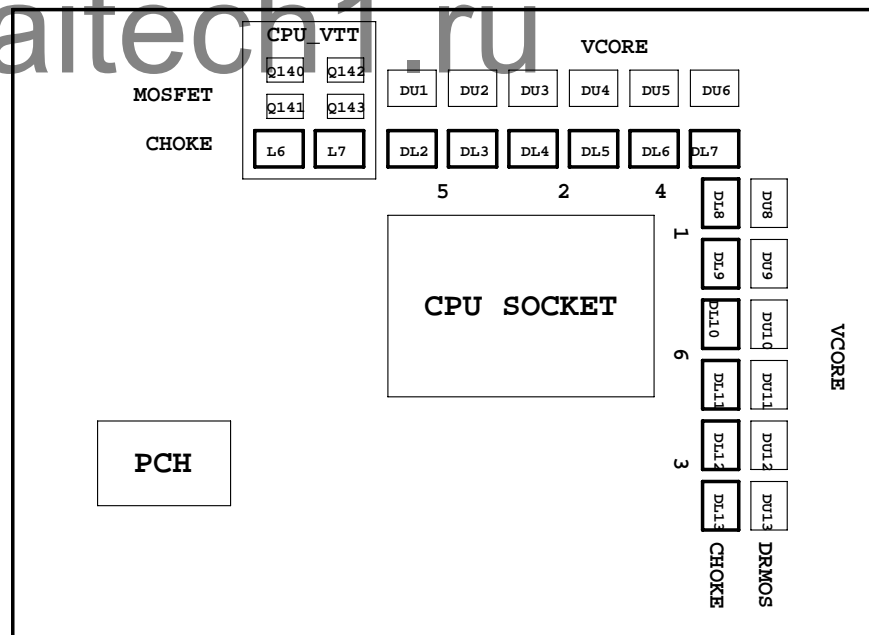
Model Name: GA-P67A-UD3P-B3 1.1

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*8 SLOT
16	PCI EXPRESS*16/*8 SWITCH
17	PCI EXPRESS*1 SLOTS X3
18	PI7C9X113SL
19	PI7C9X113SL POWER
20	PCI SLOT 1&2
21	I/O ITE8728
22	COM, -PROHOT, ESATA CONNECT
23	Dual BIOS , TPM SLB9635TT
24	ALC892
25	REAR AUDIO JACK
26	VCORE PWM_ISL6366CRZ-1
27	VCORE PWM_ISL6366CRZ-2

SHEET TITLE

28	VCORE PWM_ISL6366CRZ-3
29	DISCRETE POWER I
30	DDR_15V & VCC1_05_PCH PWM_ISL6545CBZ
31	CPU_VTT PWM_ISL6322G
32	VCCSA POWER
33	F_PANEL , F_USB , FDD
34	ATX POWER, CLOCK GEN
35	HWM,KB/MS , FAN CTRL
36	REALTEK RTL8111E
37	ESATA SE9128
38	FRONT NEC USB3.0
39	REAR NEC USB3.0
40	TABLE LIST



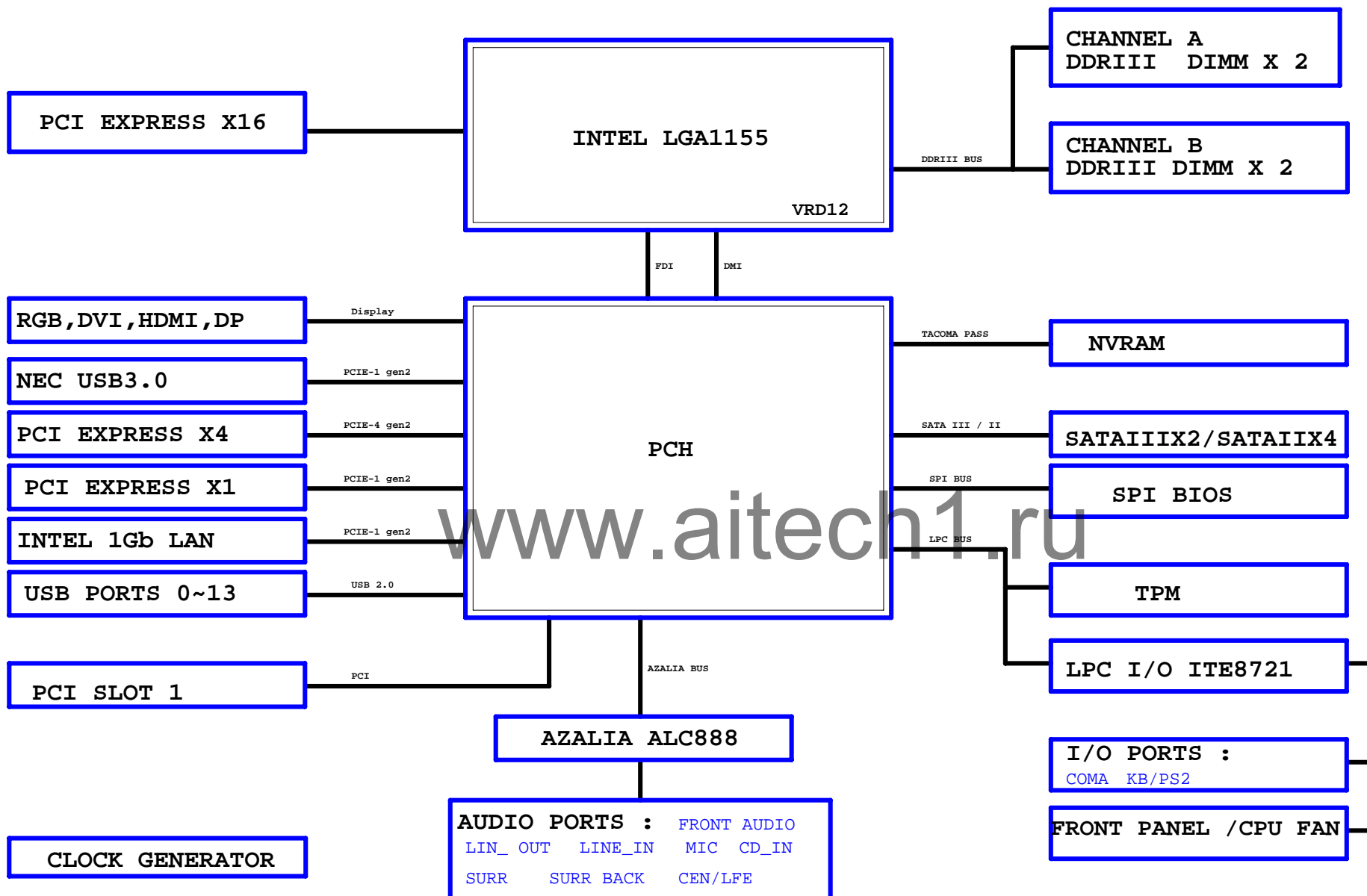
Component value change history

Data	Change Item	Reason
0.1	EVT RELEASE	
P67A-UD3R-0.1	1. ITE8728 VIN1 VCC3/VCC Detect confirm	
	2. REMOVE CMD1293	
	3. Add LGA1155 LOTOS Socket & ILM	
	4. ITE8275 怎麼上?	
	5. 注意變相的BOM上法,放大改3倍	
	6. R,C值統一	
	6. PCI-E TO PCI Bridge電壓先用1.2V,新版本CHIPS再改回1.1V	
	7. VCORE LOAD-LINE 調整	
P67A-UD3R-0.2	1. 9MP67AU3R-00-02	
P67A-UD3R-0.1	1. PCH & ITE8275 & ITE8728 & ISL6366最後版本確認	
	2. LBC13 4.7U/6 --> 10U/8	
P67A-UD3P-0.4	1. P67A-UD3R REV1.0 --> P67A-UD3P RV0.4	
	2. PWM 8 PHASE --> 12 PHASE	
P67A-UD3P-1.0A	1. ITE8275 RESET DR237 0/4 --> 22K/4	
	2. PWM_CR3-CR6 8.2K+0.01u/4	
11A-1209	1. Dual BIOS 改成 Hold pin GPIO	
	2. ALC892 --> ALC889	
11B	1. UU2,FUU1 UPD720200F1 --> UPD720200AF1	
11C-0121	1. PCB "依利安達"移除	
	2. Patch ITE8728低溫相容性和增加SVIDCLK Margin	
P67A-UD3P-B3-10A 0209	1. PCH Rev.B2 --> Rev.B3	

Circuit or PCB layout change

DATE	Change Item	Reason
2010/07/26-0.1	P67A-UD3P REV0.1修改	
P67A-UD3R-0.1	1. IO的LPCCCLK48 REF GND(參考P67A-UD3P REV0.2)	
	2. ADD文字面ON/OFF Charge , Dynamic Energy Saver後面不需要加"2" ,	
	3. F_USB 5VDUAL1鋪銅加強	
	4. REMOVE PI7C9X113SLFDE VDDCAUX	
	5. RN6下方的VIA移除一顆	
	6. 0ohm short (包含0402/0603/0805)	
	7. CLK Buffer 省略?	
	8. NEC USB3.0 PONRSTB在第一顆LDO預留電阻	
	9. UPDATE POWER PACK Footprint "Q_TDS0N8-GDS-5"	
	10. Add DRMOS保護線路,-PROCHOT OP改上此線路	
	11. ITE8275 Straping pin不能和A_WORK & B_WORK共用25MHz要加嗎?	
	12. PCH_DPWORK須做Delay 20ms	
	13. CHECK DOWN SIZE	
	14. GPIO27 Straping --> GPIO31 Straping , 注意AC2_SDOUT走T型,要修改	
	15. RN6下方的VIA移除一顆	
	16. PCH.AU38,PCH.AT40要修改內層For 3VDUAL通道	
	17. Update SATA3 library	
	18. Add 文字面"Dolby" logo	
	19. ISEN1-ISEN6 遠離NET "PWM1~6"	
	20. SVID Signle 4/12	
	21. CPU端,加強DDR15V通道	
	22. Add DR319-DR321 For DES Control	
	22. Add DQ61,DQ62,DR316-DR318 For Vcore Boot voltage=1.1V	
	23. NET SWAP "SMIB" & "-ICH_PSI"	
	24. Add EN_PH2 CONTROL , CHANGE NET p_LED1-P_LED6"	
	25. Add U18 switch for usb3.0	
2010/07/29-0.2	1. PRN1,PRN2 8P4R-0603 --> 8P4R-0402	
	2. SVID ICT移除,注意走線要同GROUP走在一起	
	3. PCB改黑色系(包含Connect)	
	4. PCIEX4 CLK Change to PCH PCIE port3	
	5. 0ohm short (包含0402/0603/0805)	
	6. DR210 SMIB位置修正	
	7. MOS_HS1、MOS_HS2與EC6、DEC1、DEC2、DEC3、L1、L2、DL4-DL9、DL12、DL13文字框距離不足1mm	
1.1	1. UPDATE ATX_2X4P , POWER PACK FOOTPRINT	
	2. ALC892 --> ALC889	

BLOCK DIAGRAM



LGA1155A

MAAA0	AV27	SA_MA[0]	SA_DQS[0]	AK3	DQSA0
MAAA1	AY24	SA_MA[1]	SA_DQS[0]	AK2	-DQSA0
MAAA2	AW24	SA_MA[2]			
MAAA3	AV23	SA_MA[3]			
MAAA4	AV23	SA_MA[3]		AJ3	MDA0
MAAA5	AT24	SA_MA[4]	SA_DQ[0]	AJ4	MDA1
MAAA6	AT23	SA_MA[5]	SA_DQ[1]	AL3	MDA2
MAAA7	AU22	SA_MA[6]	SA_DQ[2]	AL4	MDA3
MAAA8	AV22	SA_MA[7]	SA_DQ[3]	AJ2	MDA4
MAAA9	AT22	SA_MA[8]	SA_DQ[4]	AJ1	MDA5
MAAA10	AV28	SA_MA[9]	SA_DQ[5]	AL2	MDA6
MAAA11	AU21	SA_MA[10]	SA_DQ[6]	AL1	MDA7
MAAA12	AU21	SA_MA[11]	SA_DQ[7]		
MAAA13	AW32	SA_MA[12]	SA_DQS[1]	AP3	DQSA1
MAAA14	AU20	SA_MA[13]	SA_DQS[1]	AP2	-DQSA1
MAAA15	AT20	SA_MA[14]			
		SA_MA[15]			
7 -SWEA	-SWEA	AW29	SA_WE#	AN1	MDA8
7 -SCASA	-SCASA	AV30	SA_CAS#	AN4	MDA9
7 -SRASA	-SRASA	AU28	SA_RAS#	AR3	MDA10
			SA_DQ[8]	AR4	MDA11
7 SBAA0	SBAA0	AY29	SA_BS[0]	AN2	MDA12
7 SBAA1	SBAA1	AW28	SA_BS[1]	AN3	MDA13
7 SBAA2	SBAA2	AV20	SA_BS[2]	AR2	MDA14
			SA_DQ[10]	AR1	MDA15
7 -CSA0	-CSA0	AU29	SA_CS#0		
7 -CSA1	-CSA1	AV32	SA_CS#1	AW4	DQSA2
7 -CSA2	-CSA2	AW30	SA_CS#2	AW4	-DQSA2
7 -CSA3	-CSA3	AU33	SA_CS#3		
7 CKEA0	CKEA0	AV19	SA_CKE[0]	AV2	MDA16
7 CKEA1	CKEA1	AT19	SA_CKE[1]	AW3	MDA17
7 CKEA2	CKEA2	AU18	SA_CKE[2]	AV5	MDA18
7 CKEA3	CKEA3	AV18	SA_CKE[3]	AW5	MDA19
			SA_DQ[11]	AU2	MDA20
			SA_DQ[12]	AU3	MDA21
			SA_DQ[13]	AY5	MDA22
			SA_DQ[14]	AY5	MDA23
			SA_DQ[15]		
			SA_DQS[3]	AV8	DQSA3
			SA_DQS[3]	AW8	-DQSA3
7 DCLKA0	DCLKA0	AY25	SA_CK[0]	AY7	MDA24
7 -DCLKA0	-DCLKA0	AW25	SA_CK#0	AU7	MDA25
7 DCLKA1	DCLKA1	AU24	SA_CK[1]	AV9	MDA26
7 -DCLKA1	-DCLKA1	AU25	SA_CK#1	AU9	MDA27
7 DCLKA2	DCLKA2	AW27	SA_CK[2]	AV7	MDA28
7 -DCLKA2	-DCLKA2	AY27	SA_CK#2	AW7	MDA29
7 DCLKA3	DCLKA3	AV26	SA_CK[3]	AW9	MDA30
7 -DCLKA3	-DCLKA3	AW26	SA_CK#3	AY9	MDA31
			SA_DQ[16]		
			SA_DQ[17]		
			SA_DQ[18]		
			SA_DQ[19]		
			SA_DQ[20]		
			SA_DQ[21]		
			SA_DQ[22]		
			SA_DQ[23]		
			SA_DQS[4]	AV37	DQSA4
			SA_DQS[4]	AV36	-DQSA4
			SA_DQ[32]	AU35	MDA32
			SA_DQ[33]	AW37	MDA33
			SA_DQ[34]	AU39	MDA34
			SA_DQ[35]	AU36	MDA35
			SA_DQ[36]	AW35	MDA36
			SA_DQ[37]	AY36	MDA37
			SA_DQ[38]	AU38	MDA38
			SA_DQ[39]	AU37	MDA39
			SA_DQS[5]	AP38	DQSA5
			SA_DQS[5]	AP39	-DQSA5
			SA_DQ[40]	AR40	MDA40
			SA_DQ[41]	AR37	MDA41
			SA_DQ[42]	AN38	MDA42
			SA_DQ[43]	AN37	MDA43
			SA_DQ[44]	AR39	MDA44
			SA_DQ[45]	AR38	MDA45
			SA_DQ[46]	AN39	MDA46
			SA_DQ[47]	AN40	MDA47
			SA_DQS[6]	AK38	DQSA6
			SA_DQS[6]	AK39	-DQSA6
			SA_DQ[48]	AL40	MDA48
			SA_DQ[49]	AL37	MDA49
			SA_DQ[50]	AJ38	MDA50
			SA_DQ[51]	AJ37	MDA51
			SA_DQ[52]	AL39	MDA52
			SA_DQ[53]	AL38	MDA53
			SA_DQ[54]	AJ39	MDA54
			SA_DQ[55]	AJ40	MDA55
			SA_DQS[7]	AF38	DQSA7
			SA_DQS[7]	AF39	-DQSA7
			SA_DQ[56]	AG40	MDA56
			SA_DQ[57]	AG37	MDA57
			SA_DQ[58]	AE38	MDA58
			SA_DQ[59]	AE37	MDA59
			SA_DQ[60]	AG39	MDA60
			SA_DQ[61]	AG38	MDA61
			SA_DQ[62]	AE39	MDA62
			SA_DQ[63]	AE40	MDA63

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LGA1155[10SC1-F01155-01R]

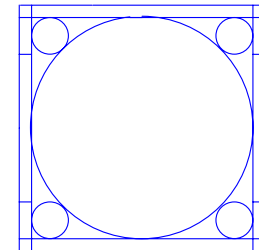
LGA1155B

MAAB0	AK24	SB_MA[0]	SB_DQS[0]	AH7	DQSB0
MAAB1	AM20	SB_MA[1]	SB_DQS[0]	AH6	-DQSB0
MAAB2	AM19	SB_MA[2]			
MAAB3	AK18	SB_MA[3]			
MAAB4	AP19	SB_MA[4]	SB_DQ[0]	AG7	MDB0
MAAB5	AP18	SB_MA[5]	SB_DQ[1]	AG8	MDB1
MAAB6	AM18	SB_MA[6]	SB_DQ[2]	AJ9	MDB2
MAAB7	AL18	SB_MA[7]	SB_DQ[3]	AJ8	MDB3
MAAB8	AY17	SB_MA[8]	SB_DQ[4]	AG5	MDB4
MAAB9	AN18	SB_MA[9]	SB_DQ[5]	AJ6	MDB5
MAAB10	AN23	SB_MA[10]	SB_DQ[6]	AJ6	MDB6
MAAB11	AU17	SB_MA[11]	SB_DQ[7]	AJ7	MDB7
MAAB12	AT18	SB_MA[12]			
MAAB13	AR26	SB_MA[13]	SB_DQS[1]	AM8	DQSB1
MAAB14	AY16	SB_MA[14]	SB_DQS[1]	AL8	-DQSB1
MAAB15	AV16	SB_MA[15]			
			SB_DQ[8]	AL7	MDB8
8 -SWEB	-SWEB	AR25	SB_WE#	AM7	MDB9
8 -SCASB	-SCASB	AK25	SB_CAS#	AM10	MDB10
8 -SRASB	-SRASB	AP24	SB_RAS#	AL10	MDB11
			SB_BS[0]	AL6	MDB12
8 SBAB0	SBAB0	AP23	SB_BS[1]	AL9	MDB13
8 SBAB1	SBAB1	AW17	SB_BS[2]	AM6	MDB14
8 SBAB2	SBAB2		SB_BS[2]	AM9	MDB15
			SB_CS#0		
8 -CSB0	-CSB0	AN25	SB_CS#1	AR8	DQSB2
8 -CSB1	-CSB1	AN26	SB_CS#2	AP8	-DQSB2
8 -CSB2	-CSB2	AL25	SB_CS#3		
8 -CSB3	-CSB3	AT26			
			SB_CKE[0]	AP7	MDB16
8 CKEB0	CKEB0	AU18	SB_CKE[1]	AR7	MDB17
8 CKEB1	CKEB1	AY15	SB_CKE[2]	AR10	MDB18
8 CKEB2	CKEB2	AW15	SB_CKE[3]	AR10	MDB19
8 CKEB3	CKEB3	AV15		AP6	MDB20
			SB_ODT[0]	AP9	MDB21
			SB_ODT[1]	AR9	MDB22
			SB_ODT[2]	AR9	MDB23
			SB_ODT[3]		
			SB_DQS[3]	AN13	DQSB3
			SB_DQS[3]	AN12	-DQSB3
			SB_CK[0]	AM12	MDB24
8 DCLKB0	DCLKB0	AL21	SB_CK#0	AM13	MDB25
8 -DCLKB0	-DCLKB0	AL22	SB_CK#1	AR13	MDB26
8 DCLKB1	DCLKB1	AK20	SB_CK#2	AR13	MDB27
8 -DCLKB1	-DCLKB1	AK20	SB_CK#3	AL12	MDB28
8 DCLKB2	DCLKB2	AL23	SB_CK#4	AL13	MDB29
8 -DCLKB2	-DCLKB2	AM22	SB_CK#5	AR12	MDB30
8 DCLKB3	DCLKB3	AP20	SB_CK#6	AP12	MDB31
8 -DCLKB3	-DCLKB3	AN21	SB_CK#7	AN28	DQSB4
			SB_CK#8	AN28	-DQSB4
			SB_DQ[32]	AR28	MDB32
			SB_DQ[33]	AR23	MDB33
			SB_DQ[34]	AL28	MDB34
			SB_DQ[35]	AL29	MDB35
			SB_DQ[36]	AP28	MDB36
			SB_DQ[37]	AP29	MDB37
			SB_DQ[38]	AM28	MDB38
			SB_DQ[39]	AM29	MDB39
			SB_DQS[5]	AP33	DQSB5
			SB_DQS[5]	AR33	-DQSB5
			SB_ECC_CB[0]		
			SB_ECC_CB[1]	AP32	MDB40
			SB_ECC_CB[2]	AP21	MDB41
			SB_ECC_CB[3]	AP35	MDB42
			SB_ECC_CB[4]	AP34	MDB43
			SB_ECC_CB[5]	AR31	MDB44
			SB_ECC_CB[6]	AR32	MDB45
			SB_ECC_CB[7]	AR34	MDB46
			SB_DQ[40]	AL33	DQSB6
			SB_DQ[41]	AM33	-DQSB6
			SB_DQ[42]		
			SB_DQ[43]	AM32	MDB48
			SB_DQ[44]	AM31	MDB49
			SB_DQ[45]	AL35	MDB50
			SB_DQ[46]	AL32	MDB51
			SB_DQ[47]	AM34	MDB52
			SB_DQ[48]	AL31	MDB53
			SB_DQ[49]	AM35	MDB54
			SB_DQ[50]	AL34	MDB55
			SB_DQ[51]		
			SB_DQ[52]	AG35	DQSB7
			SB_DQ[53]	AG34	-DQSB7
			SB_DQ[54]		
			SB_DQ[55]		
			SB_DQ[56]	AH35	MDB56
			SB_DQ[57]	AH34	MDB57
			SB_DQ[58]	AE34	MDB58
			SB_DQ[59]	AE35	MDB59
			SB_DQ[60]	AJ35	MDB60
			SB_DQ[61]	AJ34	MDB61
			SB_DQ[62]	AE33	MDB62
			SB_DQ[63]	AE33	MDB63

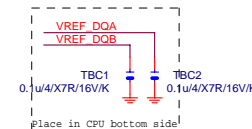
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LGA1155[10SC1-F01155-01R]

LGA1155
ILM_BP/1156/BKNI

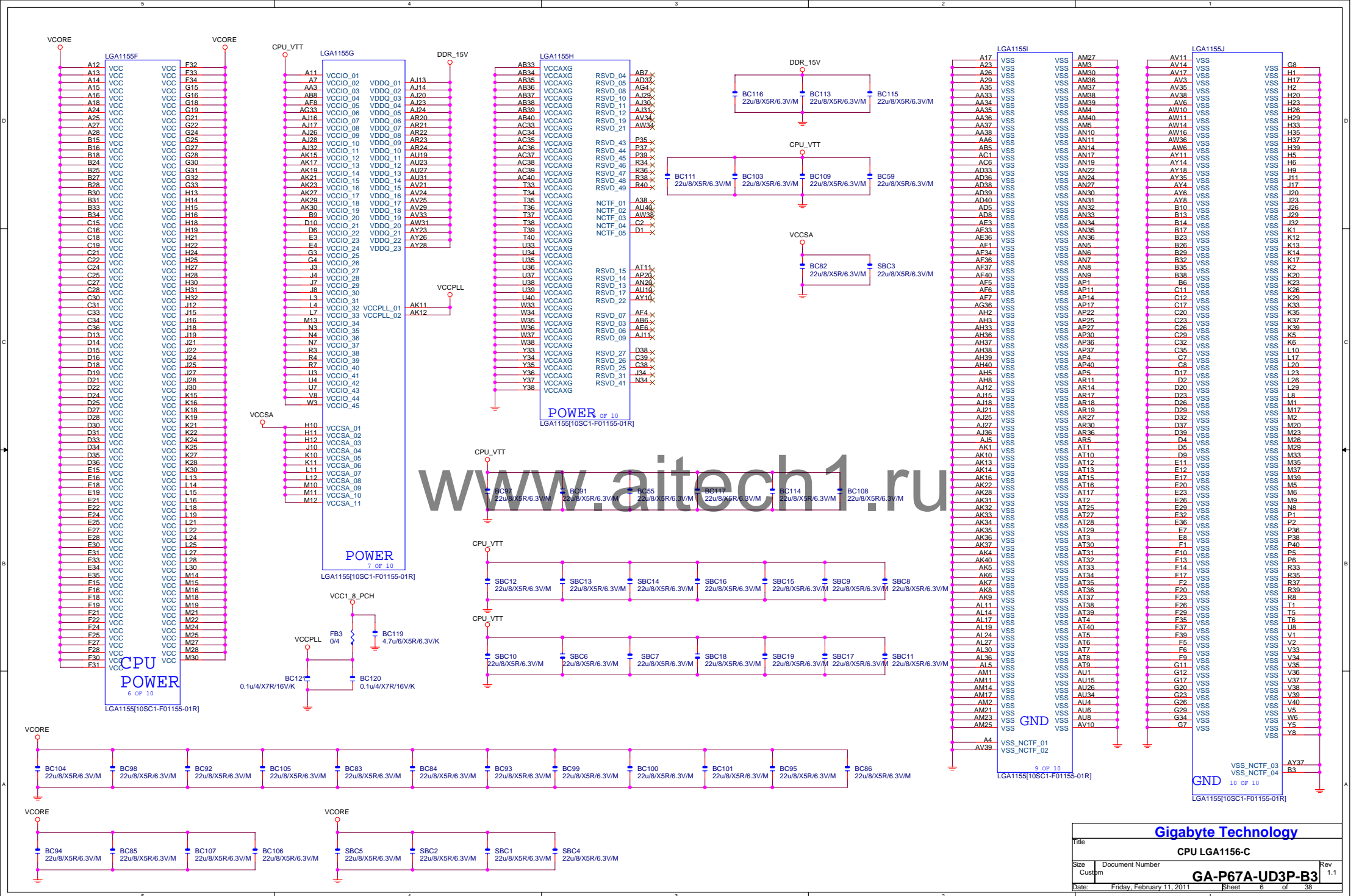
Need check the new CPU ME

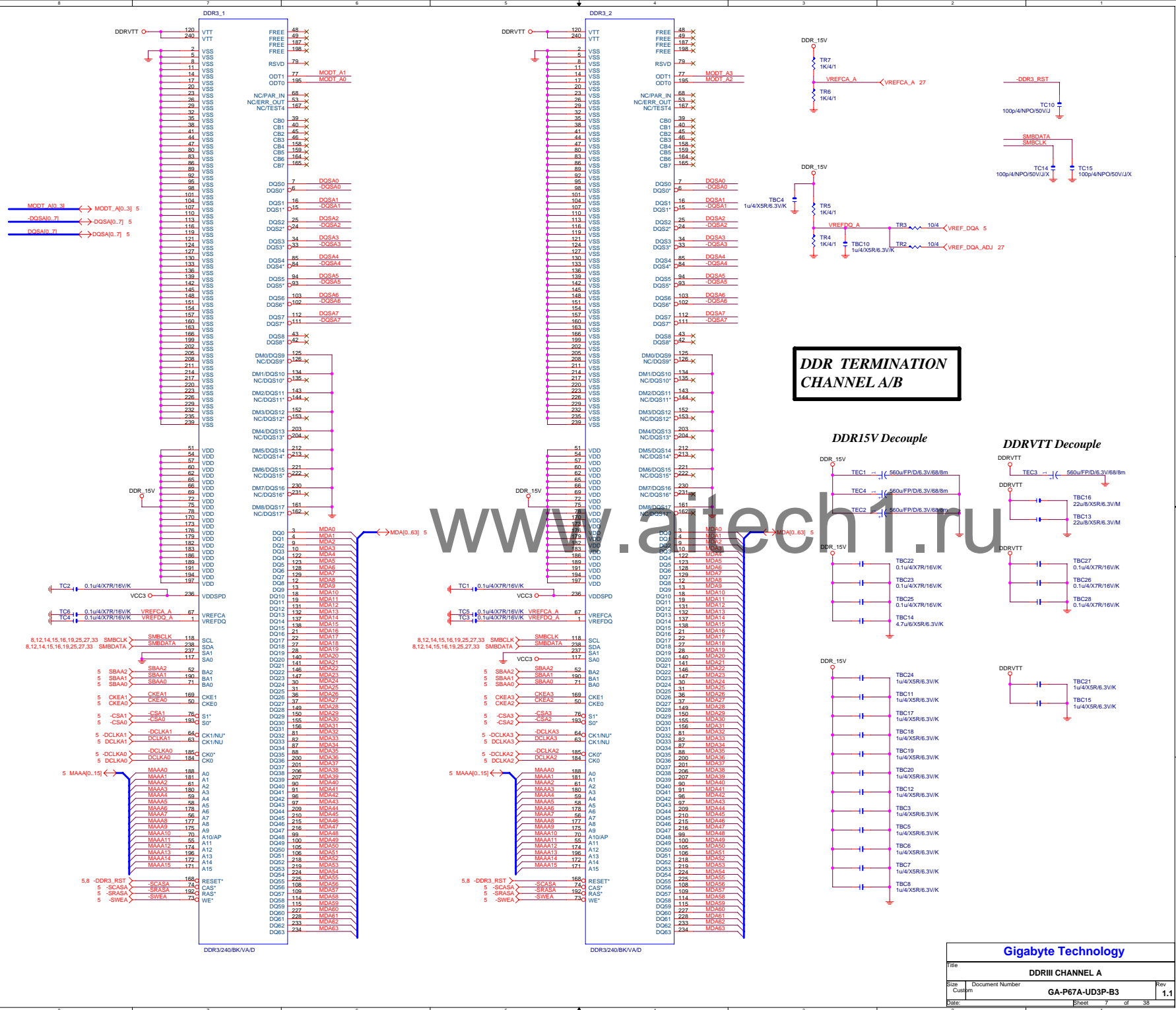


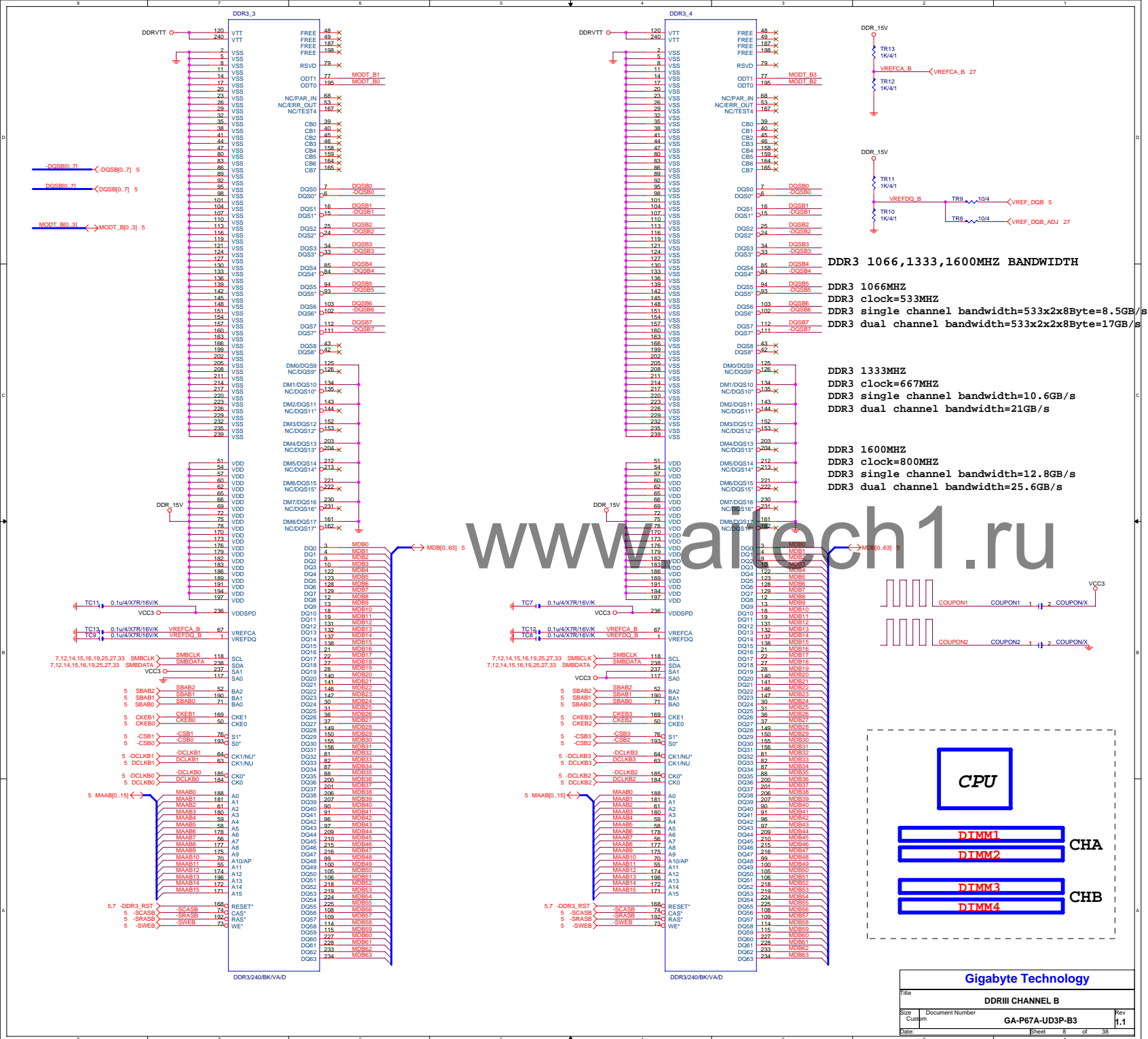
Gigabyte Technology

CPU LGA1156-B

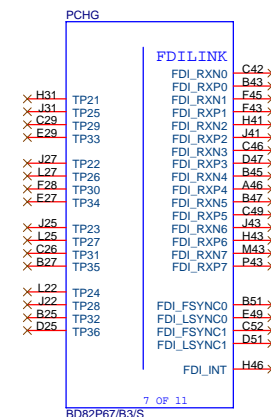
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Size	GA-P67A-UD3P-B3	1.1
Custom		
Date:	Friday, February 11, 2011	Sheet 5 of 38







PCHG



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OC[7:4]# for
Device 26
(ports 8-13)
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PCHE		
48	NV_ALE	NV_DQ0/NV_
47	NV_CLE	NV_DQ1/NV_
46	NV_RB#	NV_DQ2/NV_
45	NV_RE#_WRB0	NV_DQ3/NV_
44	NV_RE#_WRB1	NV_DQ4/NV_
43	NV_WE#_CK0	NV_DQ5/NV_
42	NV_WE#_CK1	NV_DQ6/NV_
41		NV_DQ7/NV_
40		NV_DQ8/NV_
39		NV_DQ9/NV_
38		NV_DQ10/NV_
37		NV_DQ11/NV_
36		NV_DQ12/NV_
35		NV_DQ13/NV_
34		NV_DQ14/NV_
33		NV_DQ15/NV_
32		
31		NV_C
30		NV_C
29		NV_C
28		NV_C
27		
26		NV_D
25		NV_D
24		
23		NV_RCO
22		
21		
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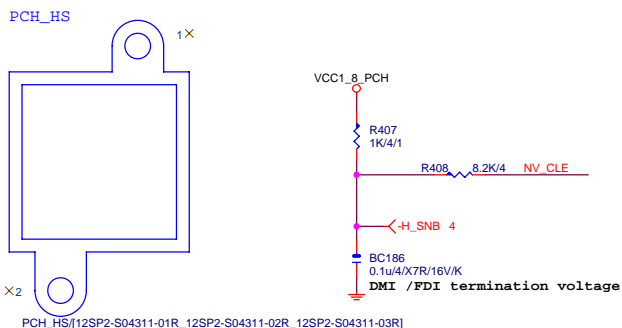
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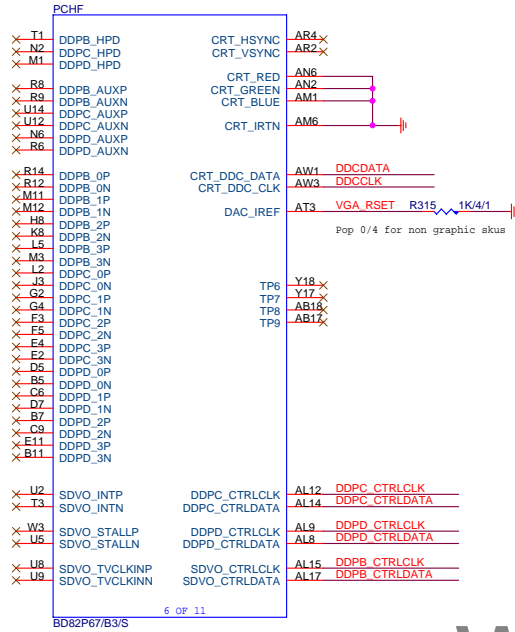
NVRAM

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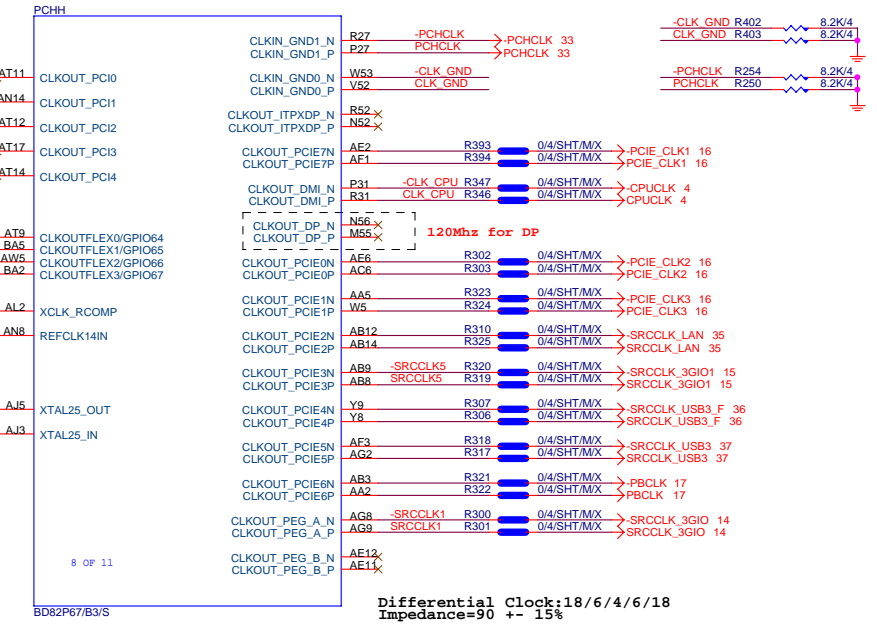
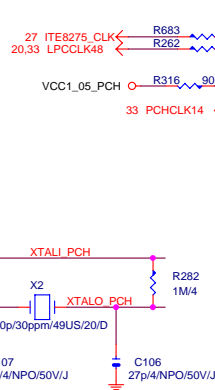
RD82P67/R3/S

PCIEX1:16/5/5/5/16 (breakout min 8/4/4/4/8)
Impedance=80 +- 17.5%





Flex0,2 : 33MHZ
Flex1,3 : 27/14/24/48/25MHZ



Strapping Signals

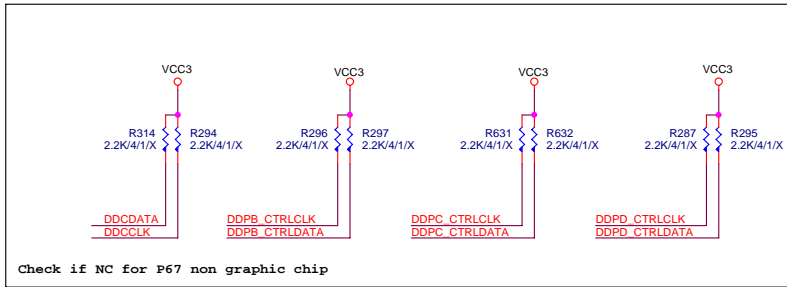
Name	Type	Recommendations	Reason/Impact
SPKR	I	Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 5.2k-10k Ohm weak pull-up resistor.	
INT3_3V	I	Do not pull low.	
GNT2# / GNT3# / GNT55	I/O	Default Mode: Internal pull-up. Top Block Swap Mode: Connect to ground with 4.7k Ohm weak pull-down resistor.	
SATA1GP / GPIO19, GNT1#	I/O	Default (SPI) Left both SATA1GP/GPIO19 and GNT1# Floating. No pull up required. Boot from PCI Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor. Leave GNT1# Floating. Boot from LPC Connect both SATA1GP/GPIO19 and GNT1# to ground with 1k Ohm pull-down resistor.	If LPC is selected BIOS may still be placed on LPC, but all platforms with PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GBE LAN.
GNT2# / GPIO53	I/O	Do not pull low.	ESI strap for server platform ONLY
HDA_SDO	I/O	Default Do not pull high. Disable ME in Manufacturing Mode Connect to VccBusHDA with 1k Ohm pull-up resistor through a jumper.	Flash descriptor: Override
SPI_MOSI	I/O	Internal weak pull down. Do not pull high.	DMI RX Termination Voltage
DF_TVS	I/O	Internal weak pull up. Do not pull low.	DMI termination voltage
HDA_SYNC	I/O	Internal weak pull down. Do not pull up.	On die PLL VR voltage selector
GPIO15	I/O	Enable TLS: Pull up with 1k Ohm to VccSus3.3. Default (Disable TLS): Leave NC. Internal pull down.	TLS confidentiality
GPIO8	I/O	BTM Leave floating. Do not pull low. FCIM Pull low with 1k Ohm to ground.	FCIM. Can be override by softstrap through ME.
GPIO28	I/O	Internal weak pull up. Do not pull low.	On die PLL voltage regulator
SATA2GP / GPIO36	I/O	Internal weak pull down. Do not pull high.	
SATA3GP / GPIO37	I/O	Internal weak pull down. Do not pull high.	

GP29 , 35 , 36 , 37 power on with 3.3V pluse

GP8 always Hi without PU

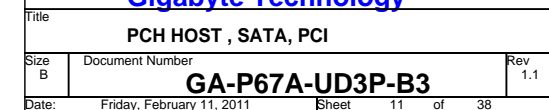
GP20 with pluse during power on & reset

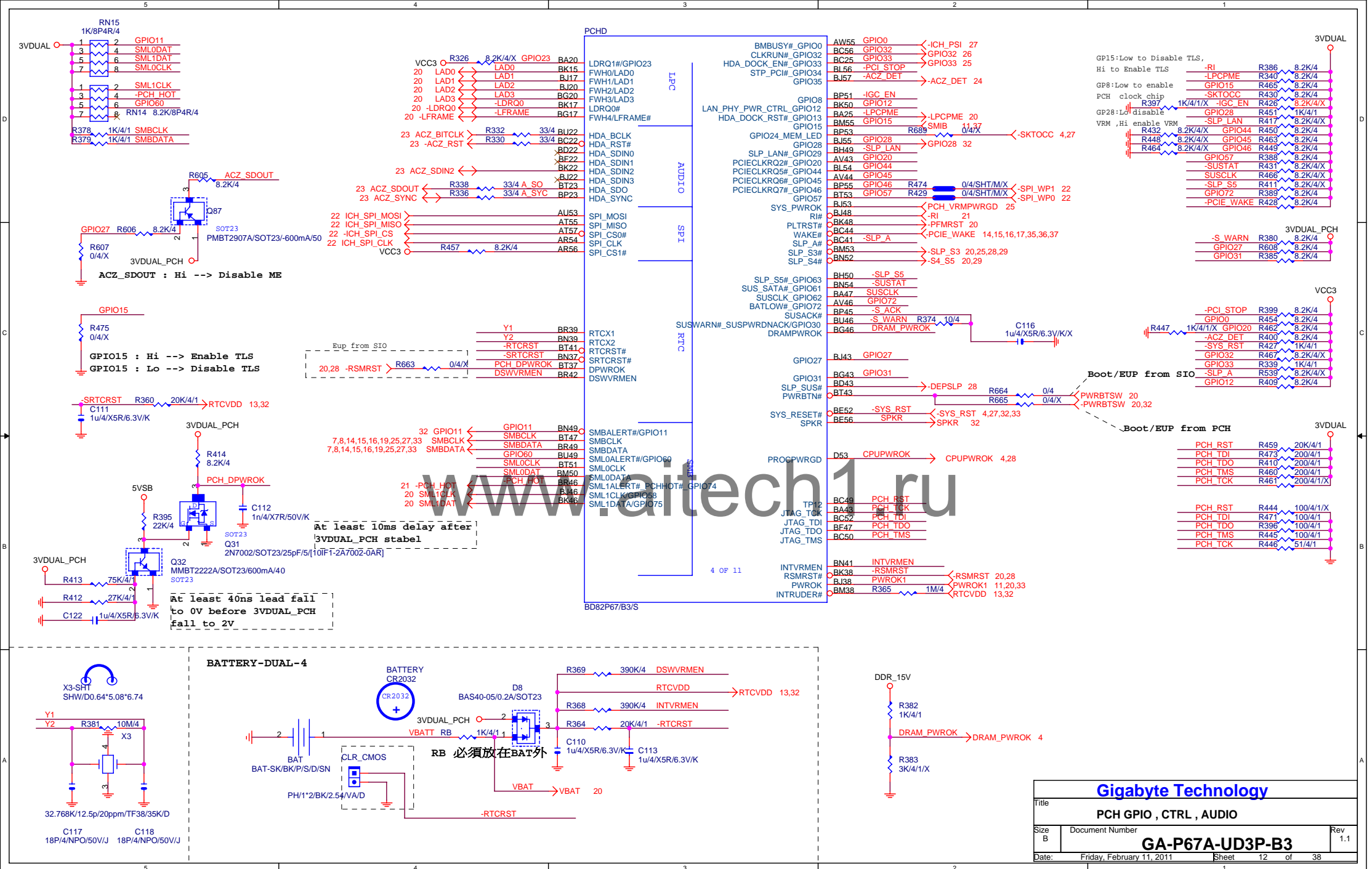
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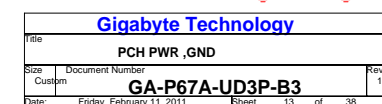


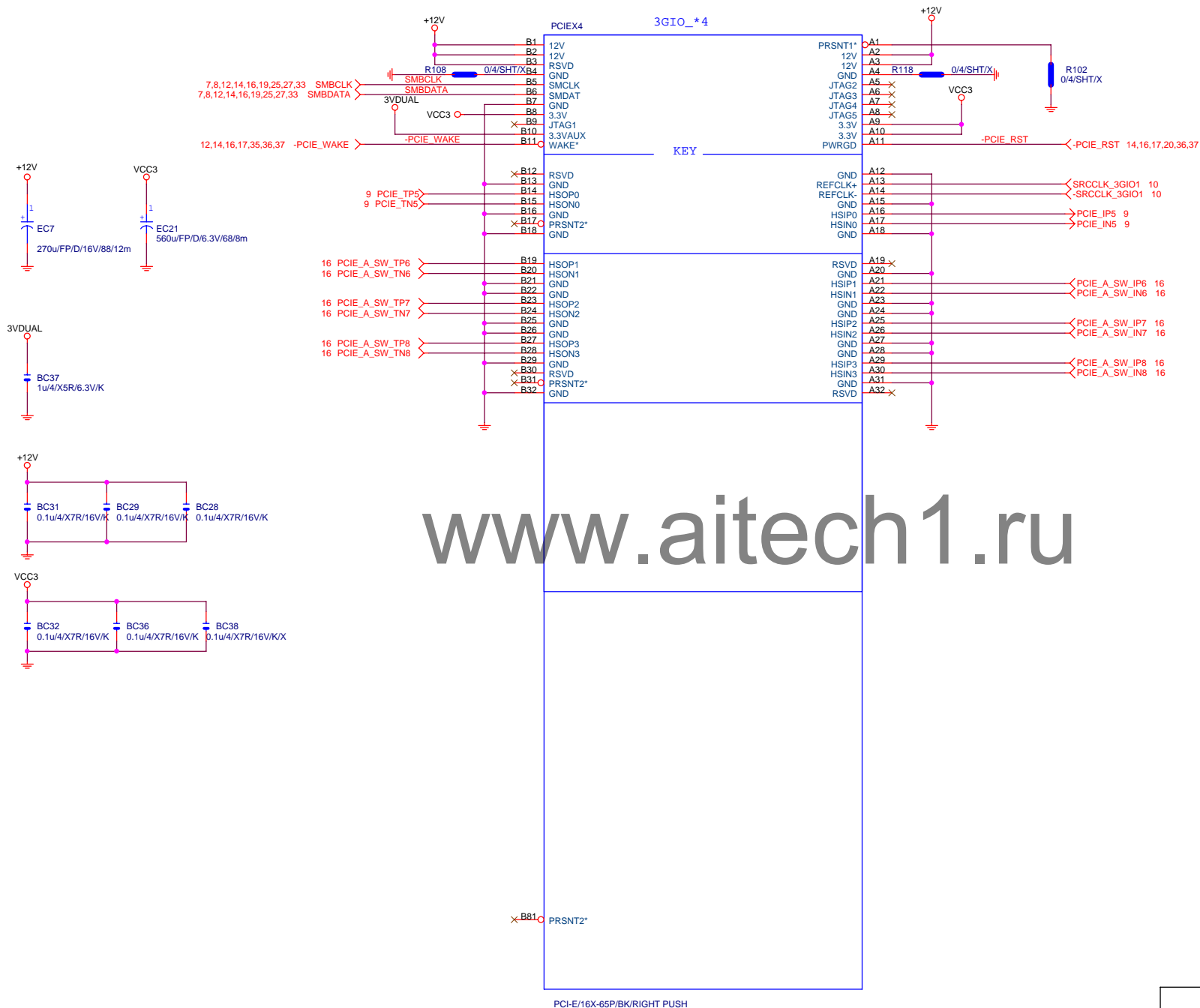
Gigabyte Technology		
Title: PCH DISPLAY ,CLK BUFFER		
Size: Custom	Document Number: GA-P67A-UD3P-B3	Rev: 1.1
Date: Friday, February 11, 2011	Sheet: 10	of 38

PCHC



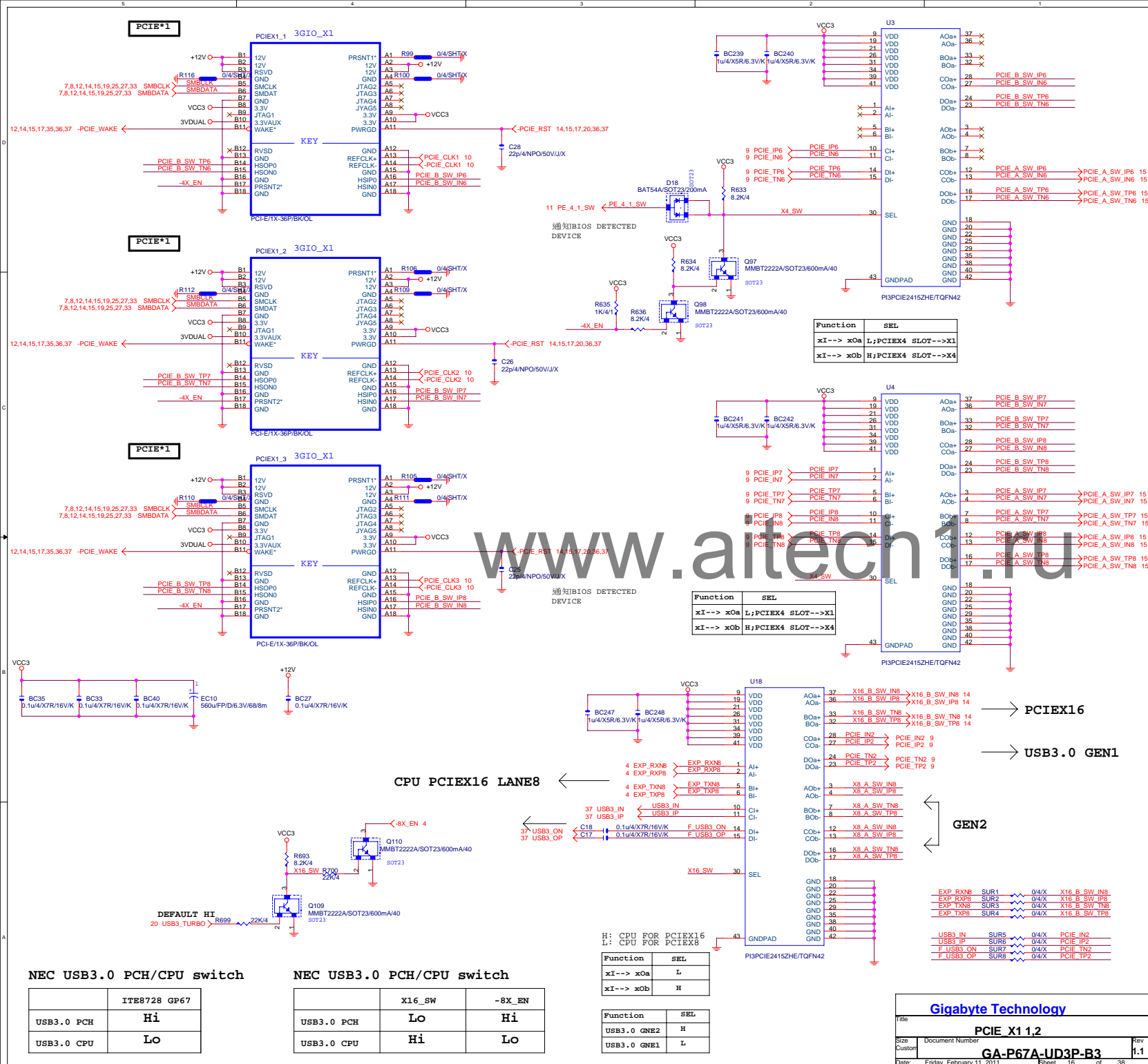






PCI-E/16X-65P/BK/RIGHT PUSH

Gigabyte Technology			
Title			
PCI EXPRESS X 4 PORT			
Size	Document Number	Rev	
Custom	GA-P67A-UD3P-B3	1.1	
Date:	Friday, February 11, 2011	Sheet	15 of 38



NEC USB3.0 PCH/CPU switch

	ITR8728 GP67
USB3.0 PCH	Hi
USB3.0 CPU	Lo

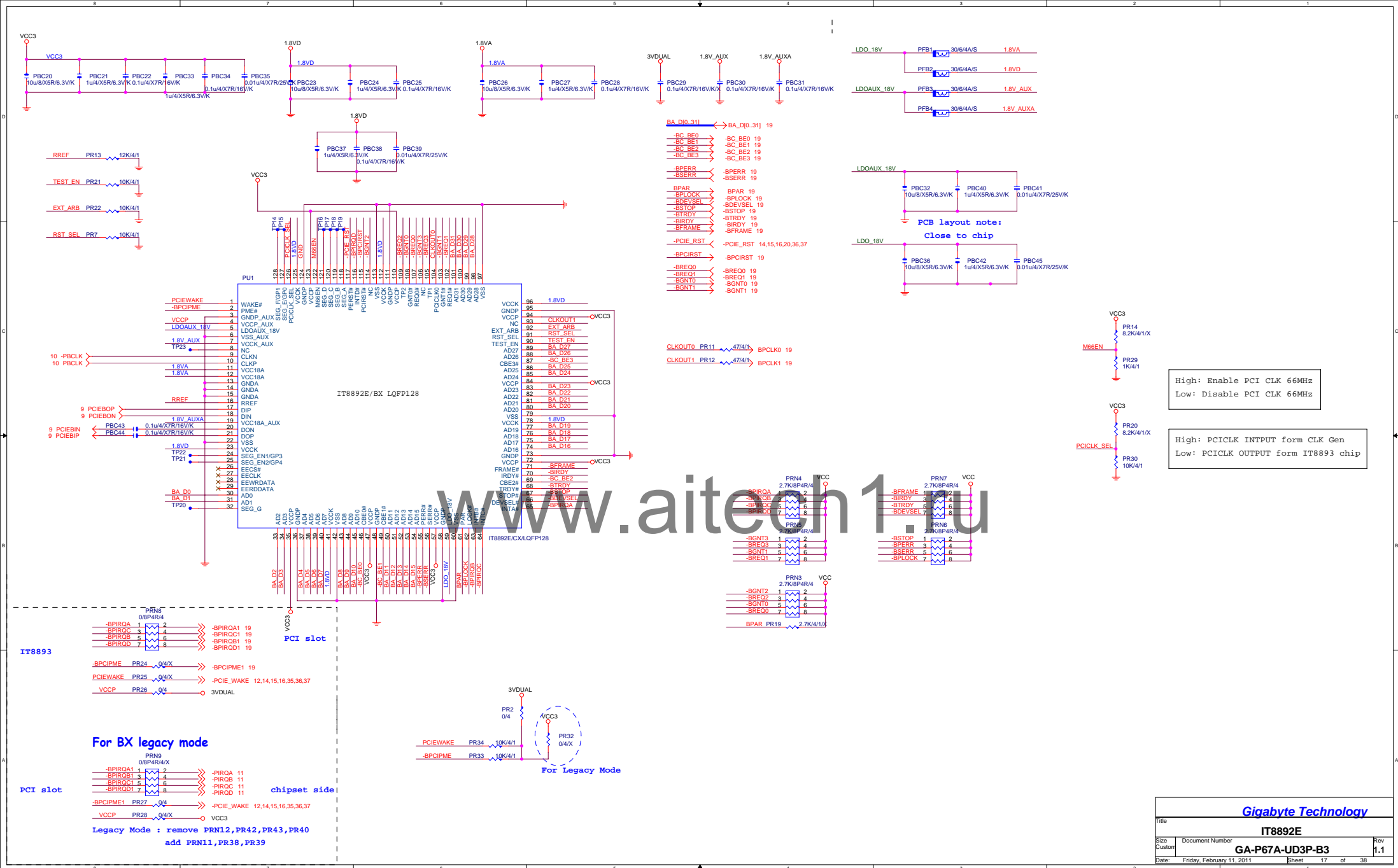
NEC USB3.0 PCH/CPU switch

	X16_SW	-8X_EN
USB3.0 PCH	Lo	Hi
USB3.0 CPU	Hi	Lo

Function	SEL
xi--> x0a	L
xi--> x0b	H

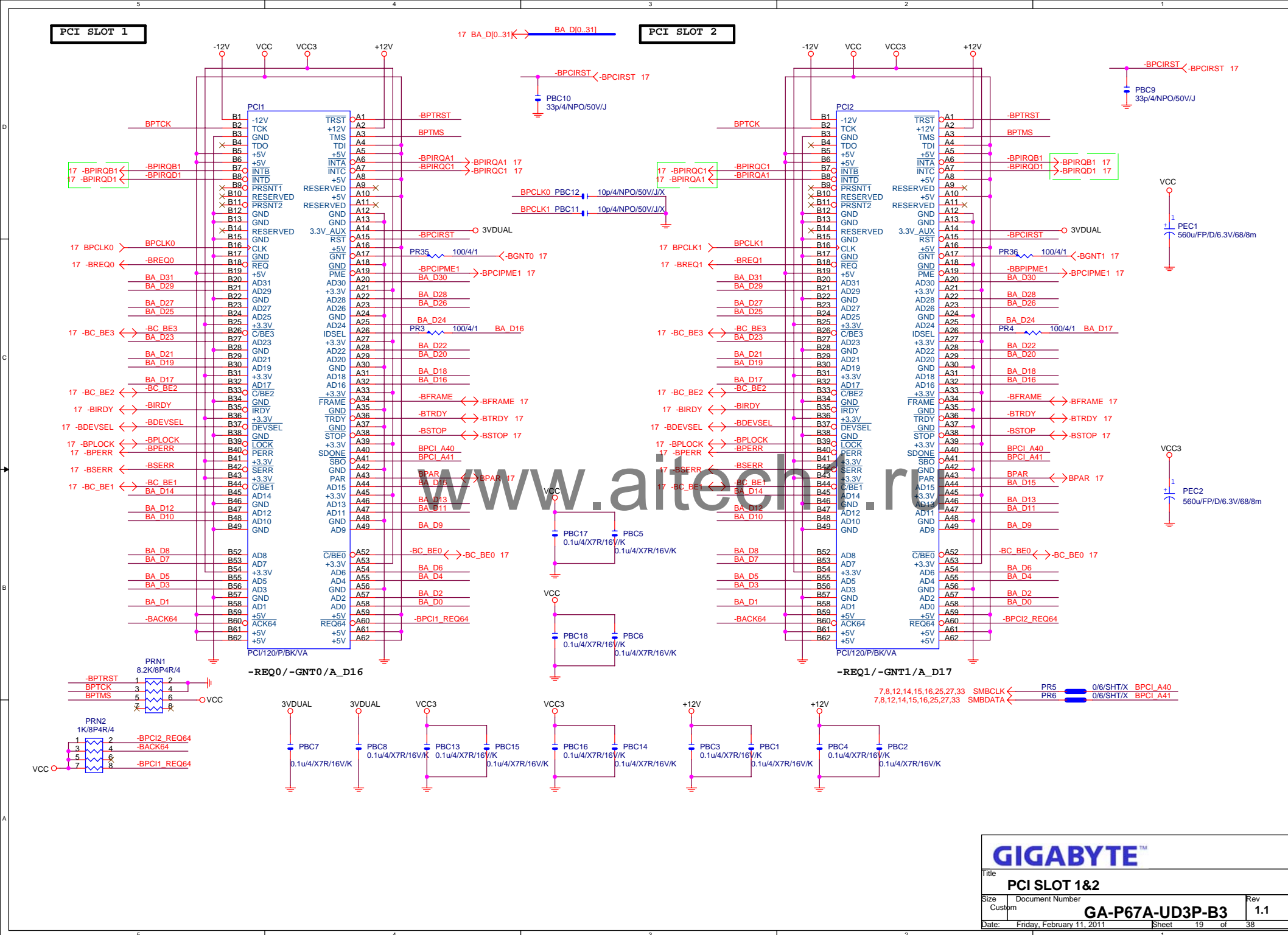
Function	SEL
USB3.0 QNE2	H
USB3.0 QNE1	L

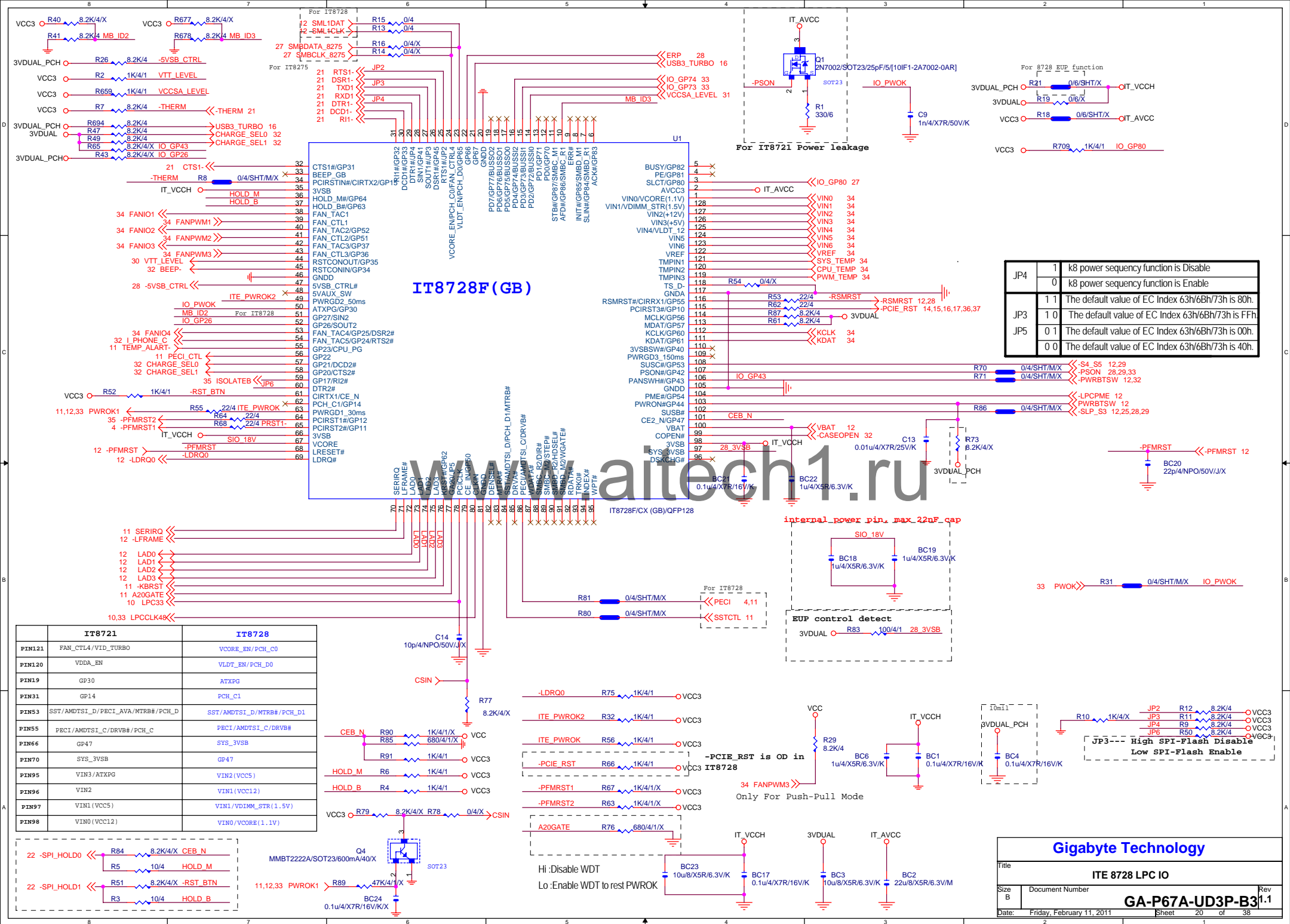
Gigabyte Technology		
PCIE X1 1.2		
File	Document Number	Rev
Size	Custom	GA-P67A-UD3P-B3
Date	Friday, February 11, 2011	1.1
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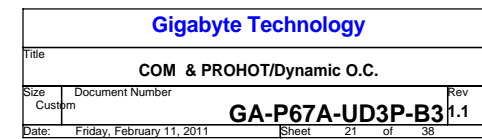
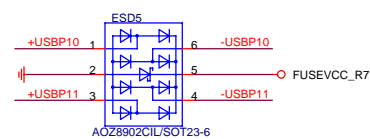
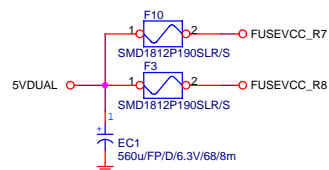
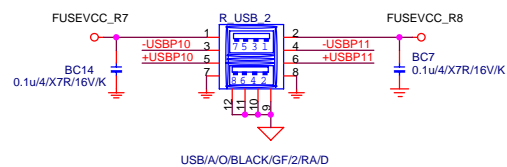
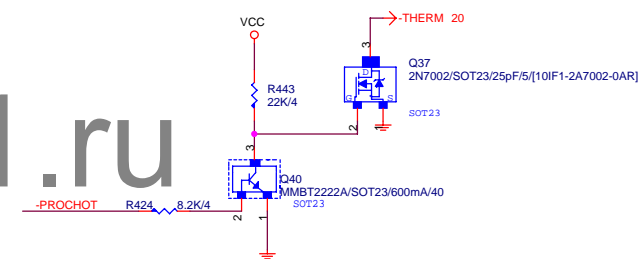
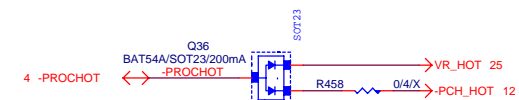
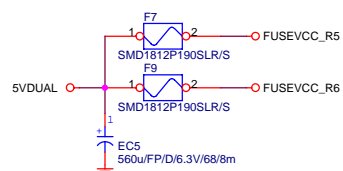
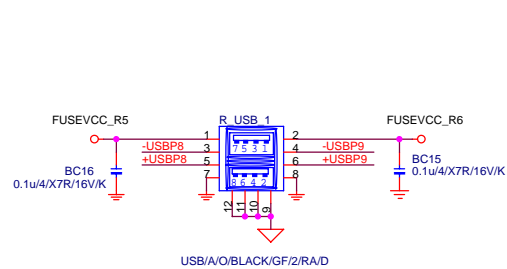
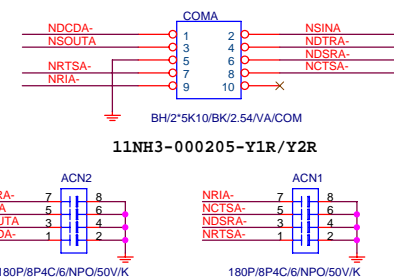
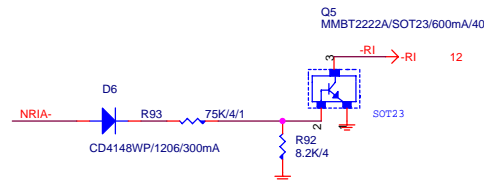
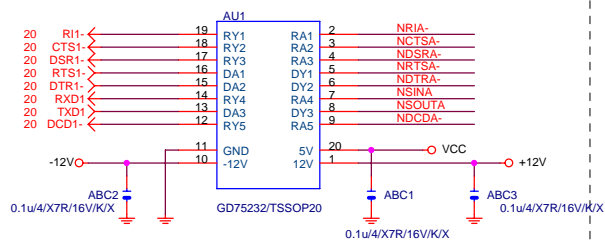


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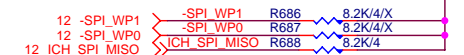
Gigabyte Technology			
Title			
PCI SLOT 1, 2			
Size	Document Number		Rev
Custom	GA-P67A-UD3P-B3		1.1
Date:	Friday, February 11, 2011		Sheet 18 of 38



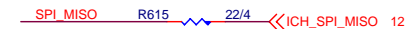




MOSI For DMI RX Termination Voltage



Default int pull up



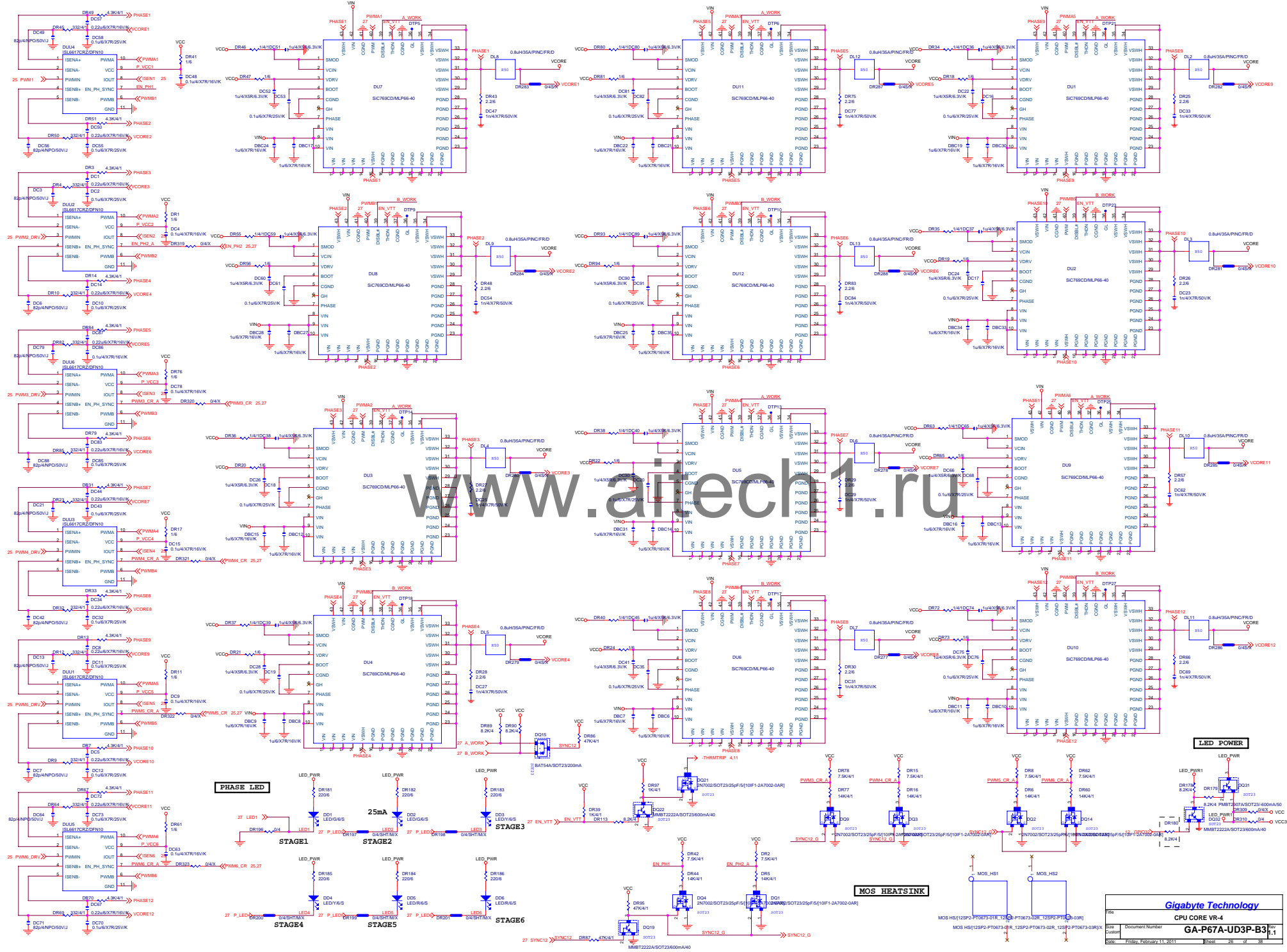
BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

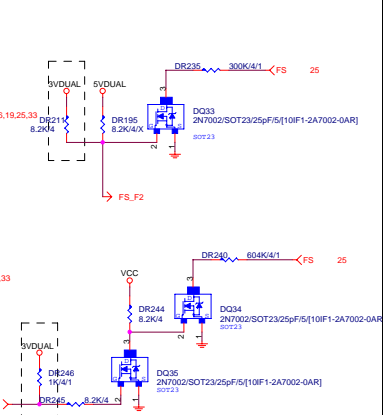
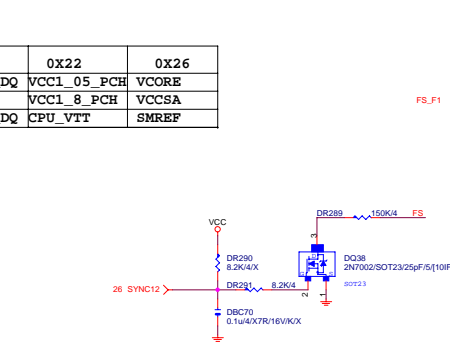
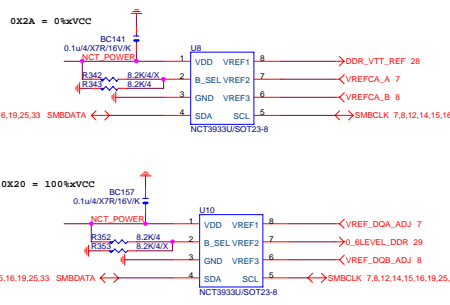
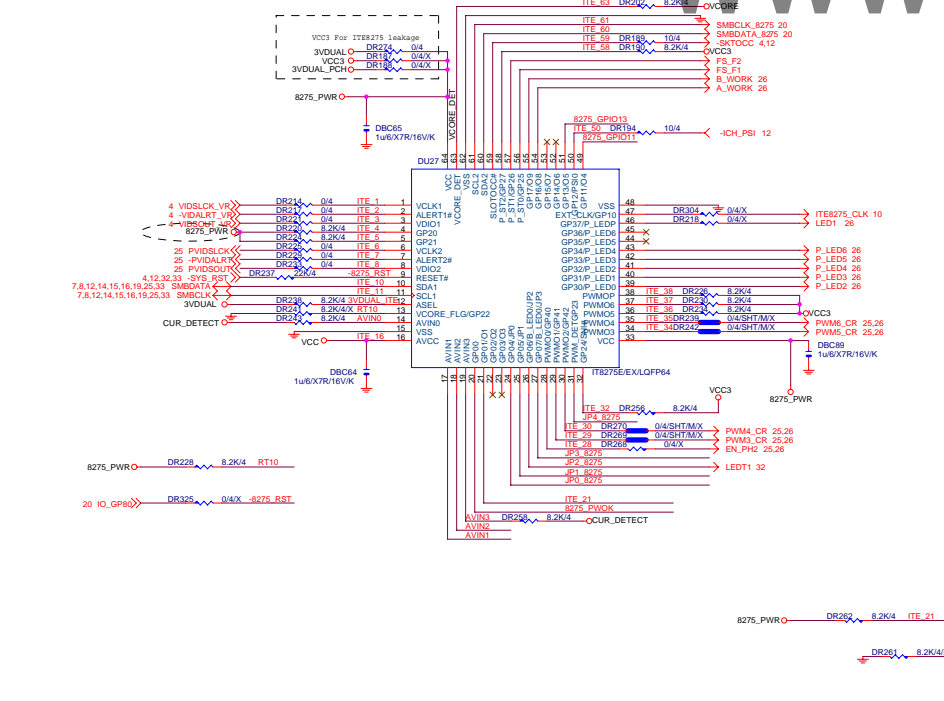
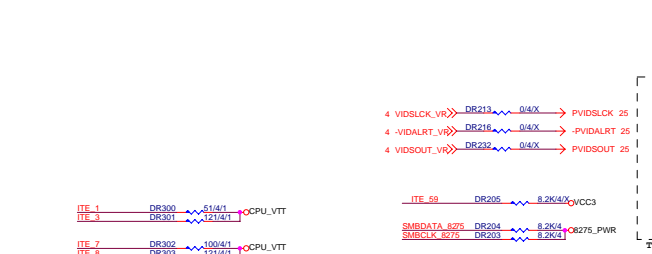
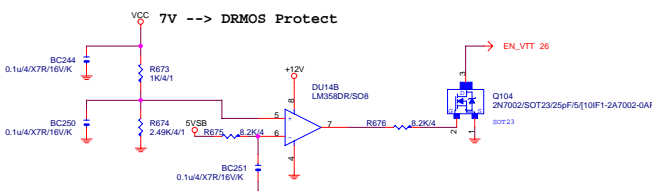
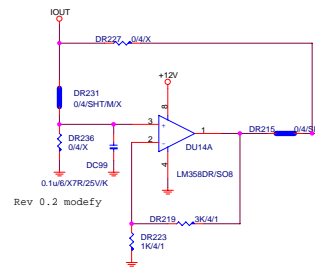
1 means floating
0 means PD 1K

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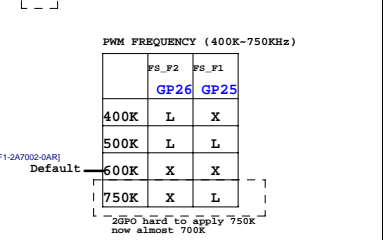
Gigabyte Technology

Title	BIOS		
Size Custom	Document Number	GA-P67A-UD3P-B3	Rev 1.1
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up6262	0X2A	0X20	0X22	0X26
VREF1	DDRVTT	VREF_DDRA_DQ	VCC1_05_PCH_OV	VCORE
VREF2	VREF_DDRA_CA	DDR15V	VCC1_8_PCH	VCCSA
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	CPU_VTT	SMREF



PWM FREQUENCY (400K-750KHz)

	F8_F2	F8_F1
GP26	GP25	
400K	L	X
500K	L	L
600K	X	X
750K	X	L

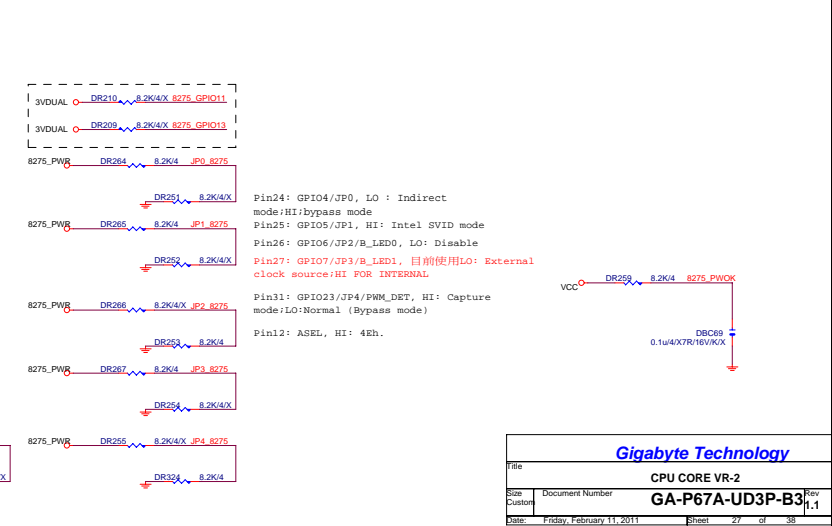
Default

250P hard to apply 750K now almost 700K

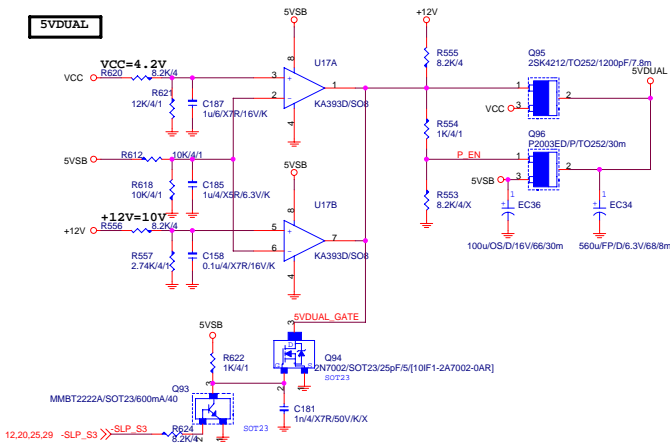
PWM FREQUENCY (200K-375KHz)

	ITB8275	ITB8275
GP26	GP25	
200K	L	H
250K	L	L
300K	H	H
375K	H	L

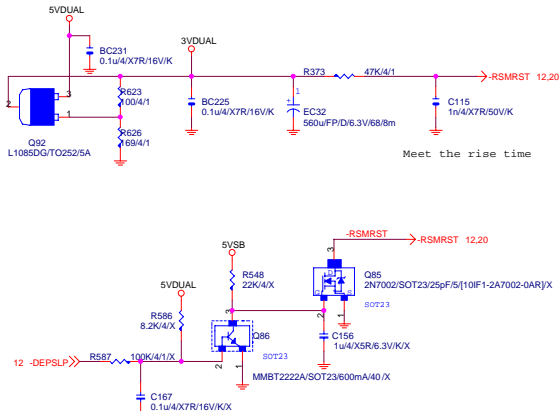
Default



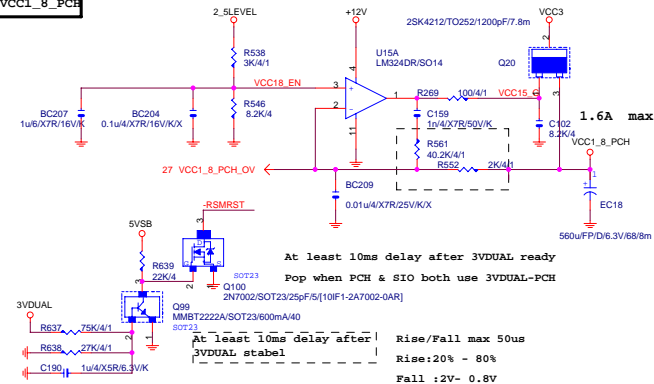
5VDUAL



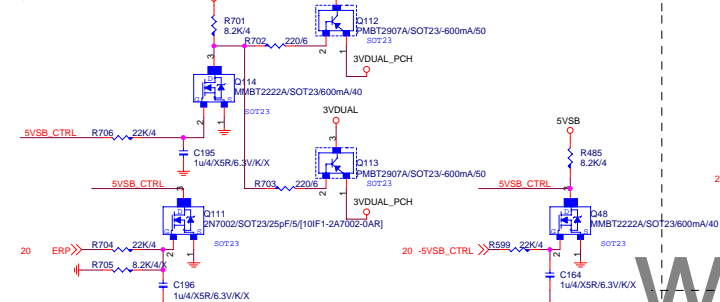
3VDUAL



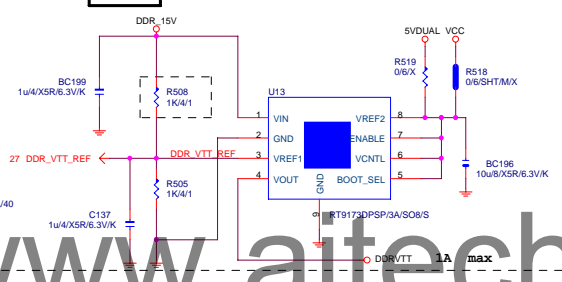
VCC1_8_PCH



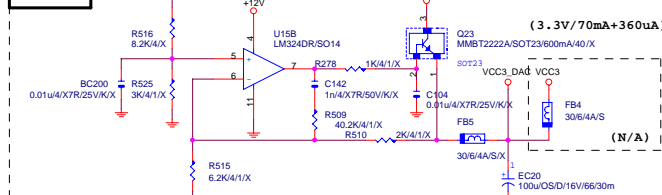
I/O ErP Control



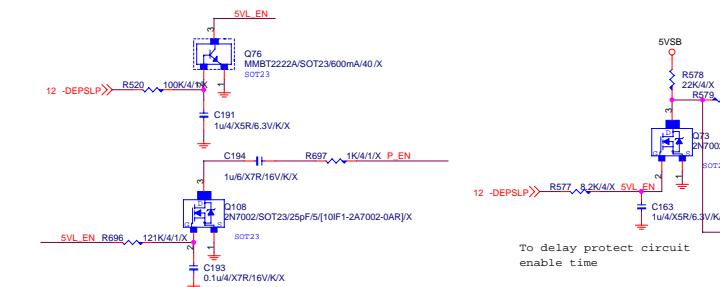
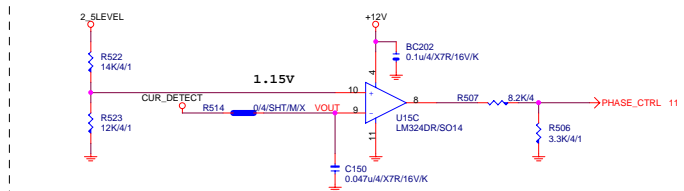
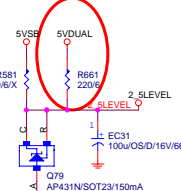
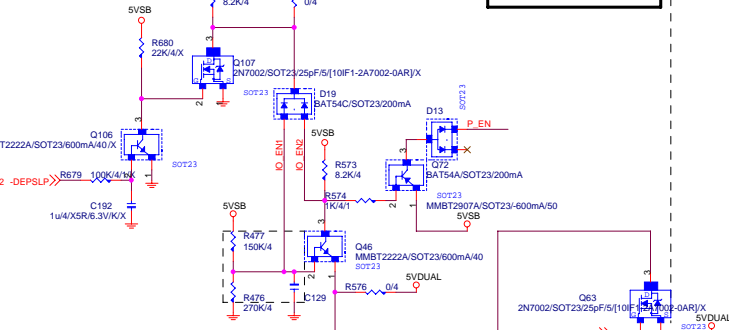
DDR_VTT



VCC3_DAC



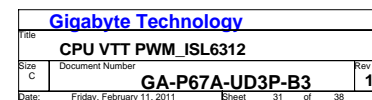
5VDUAL SHORT PROTECT

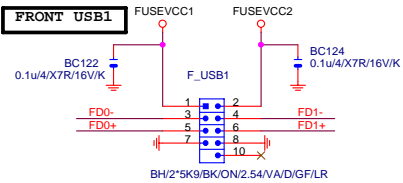


Title		DDR_15V	
Size	Document Number	Rev	
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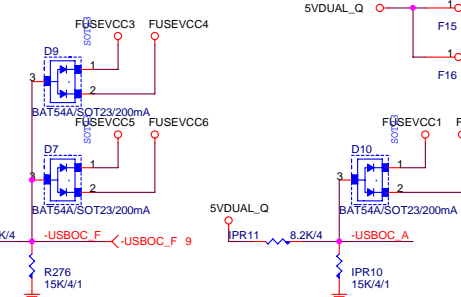
VCC_SA





i_phone charger circuit

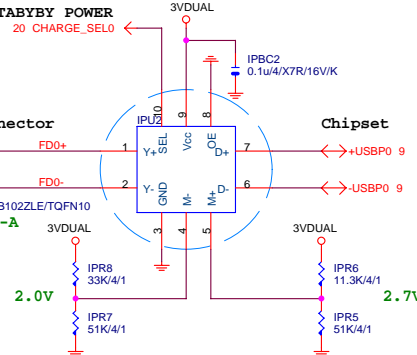
DEFAULT H, STABBY POWER



20 CHARGE_SEL0

USB connector

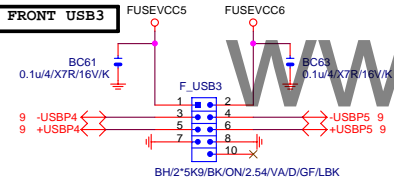
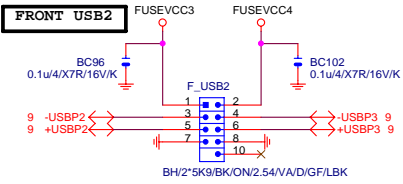
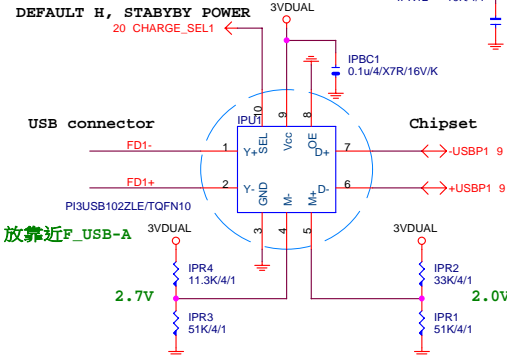
放靠近F_USB-A



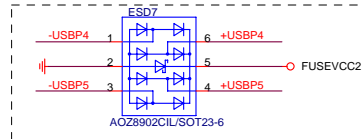
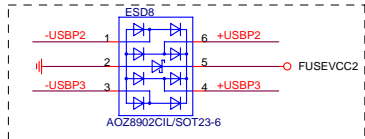
DEFAULT H, STABBY POWER

USB connector

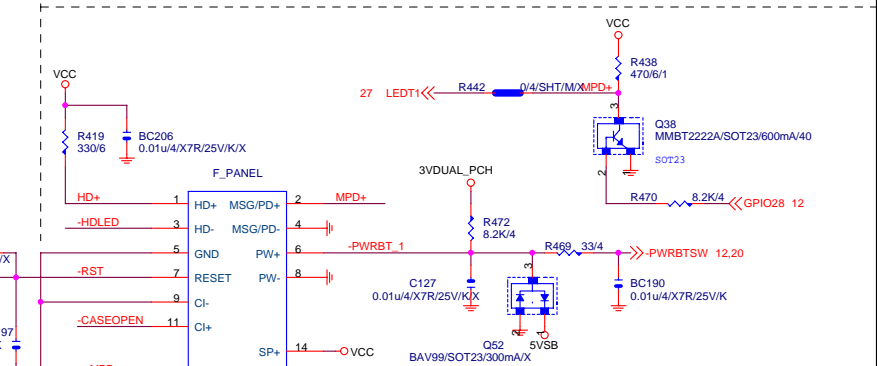
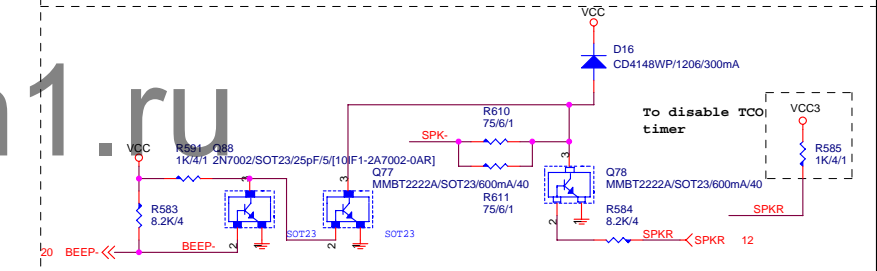
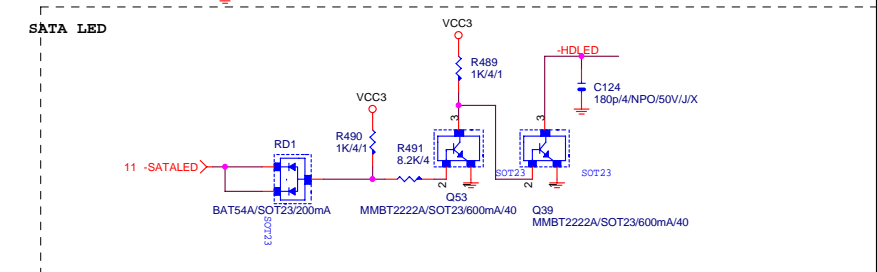
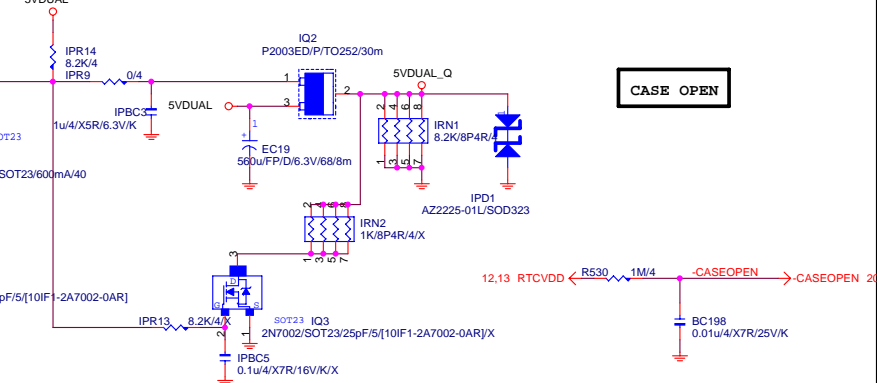
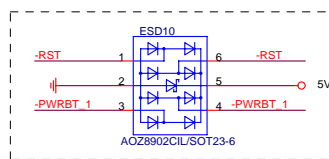
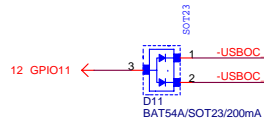
放靠近F_USB-A



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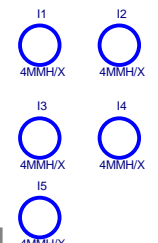
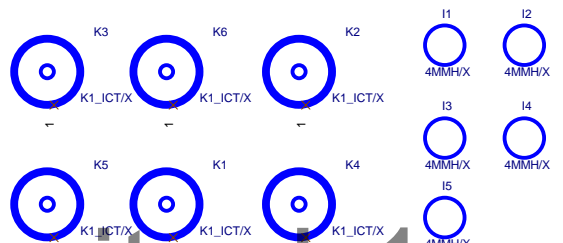
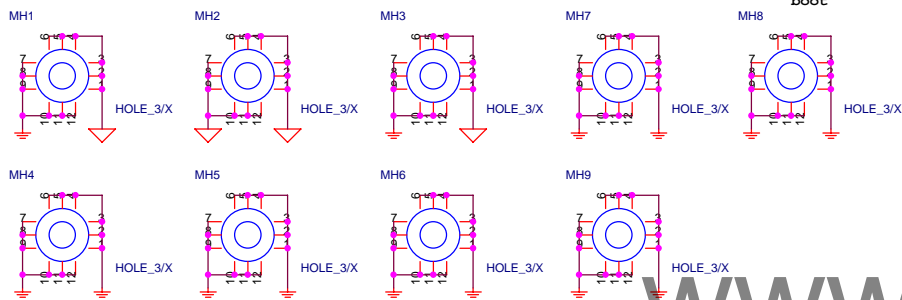
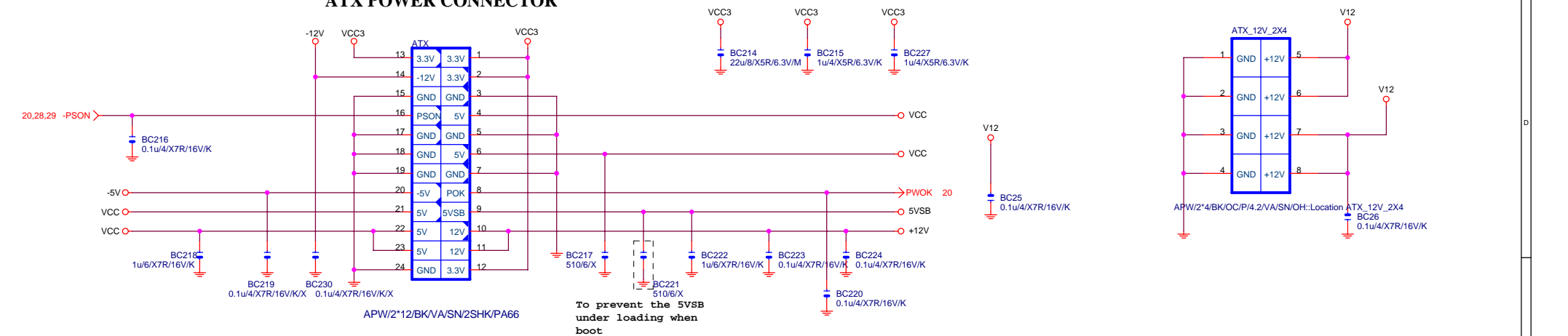


F_USB POWER PROTECT

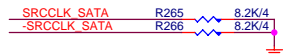


Gigabyte Technology			
Title			
FF, F_USB, USB PWR, FDD, BZ			
Size			
Custom			
Document Number			
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Rev			
1.1			

ATX POWER CONNECTOR



CLK GEN CK505



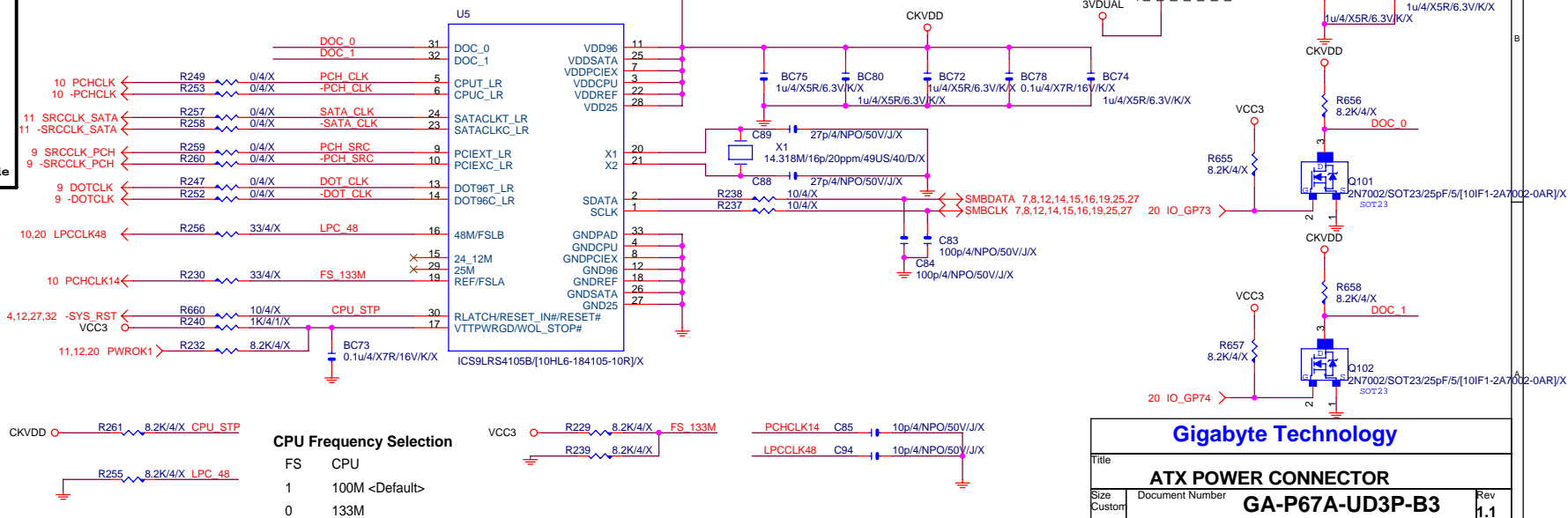
Mount for integrated clock Generation Mode



Mount for non-graphics skus



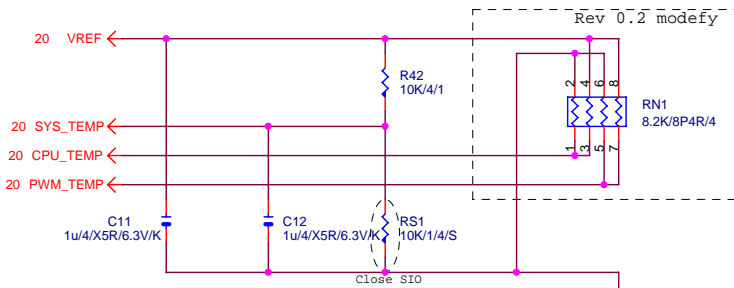
R102 short to GND in non graphic SKU



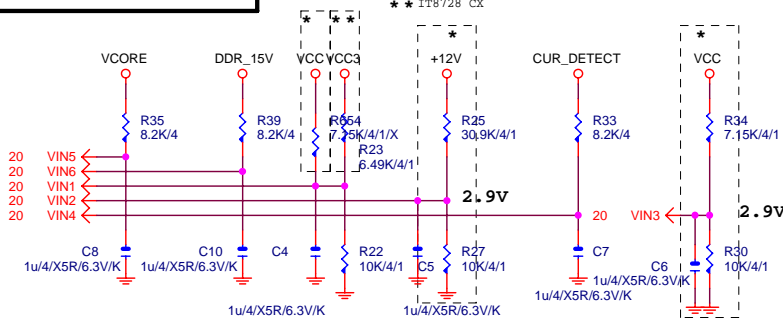
Gigabyte Technology

Title		
ATX POWER CONNECTOR		
Size	Document Number	Rev
Custom	GA-P67A-UD3P-B3	1.1
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TEMP H/W MONITOR

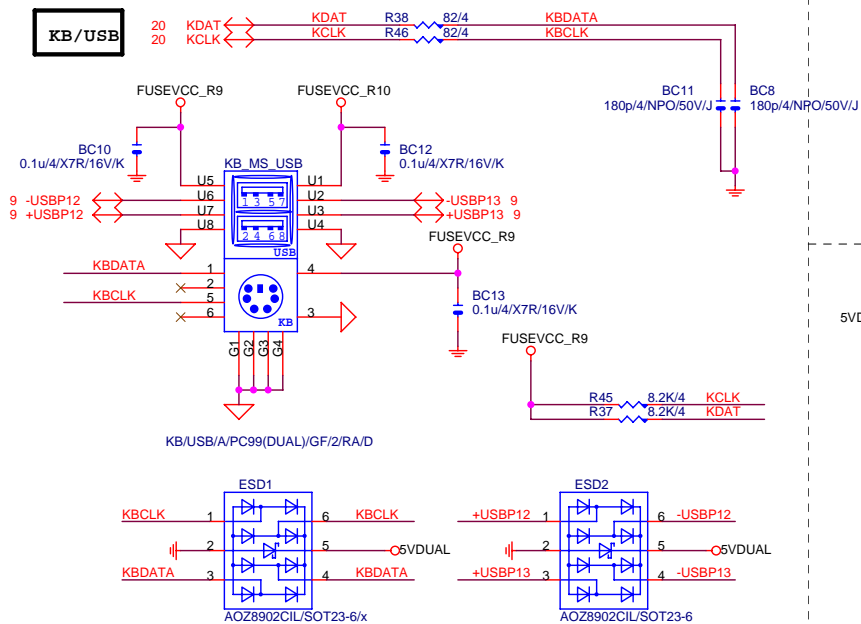


VOLTAGE-- H/W MONITOR

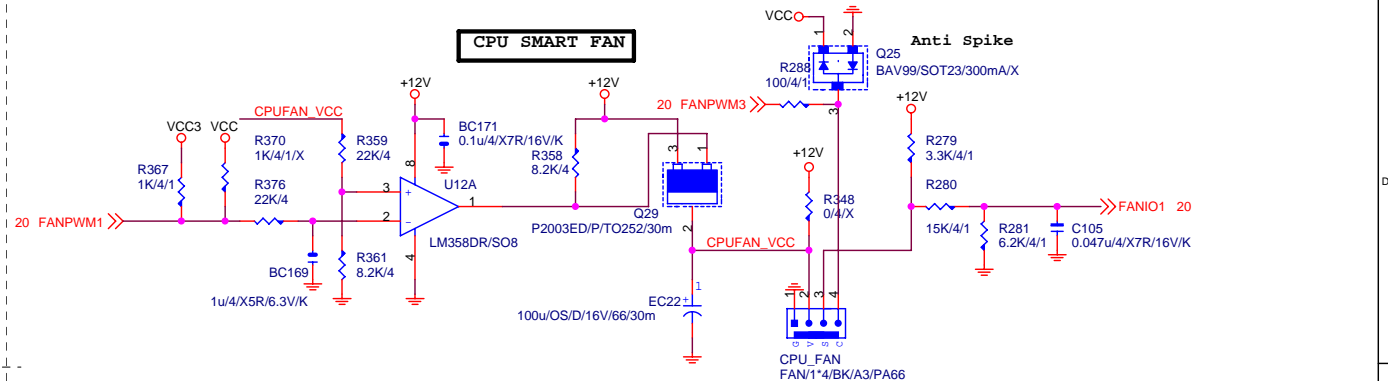


The division voltage of VIN2 & VIN3 must be around 2.9V

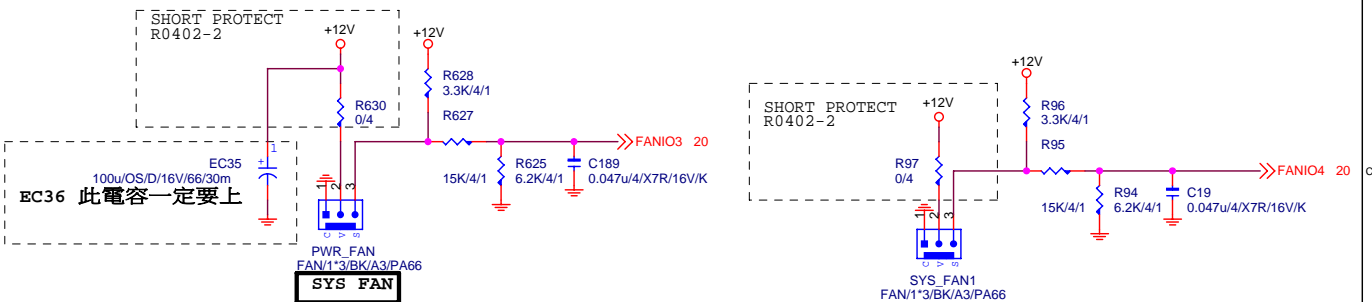
KB/USB



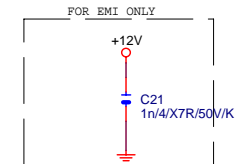
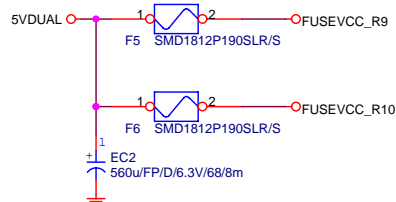
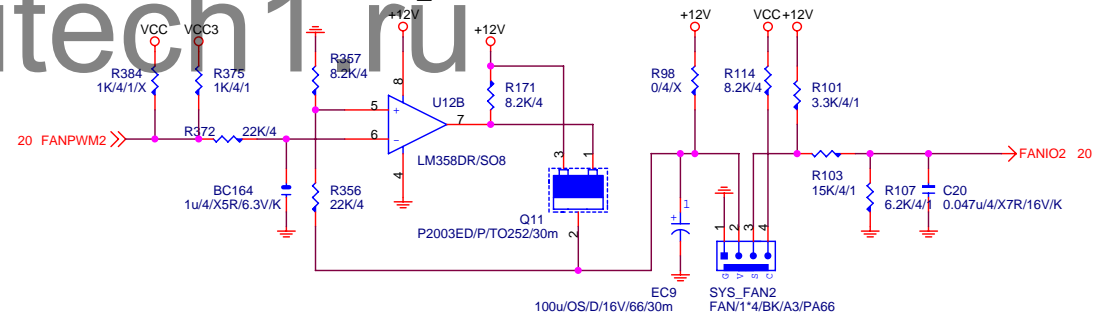
CPU SMART FAN



SYS FAN



```
Linear SYS_FAN
```



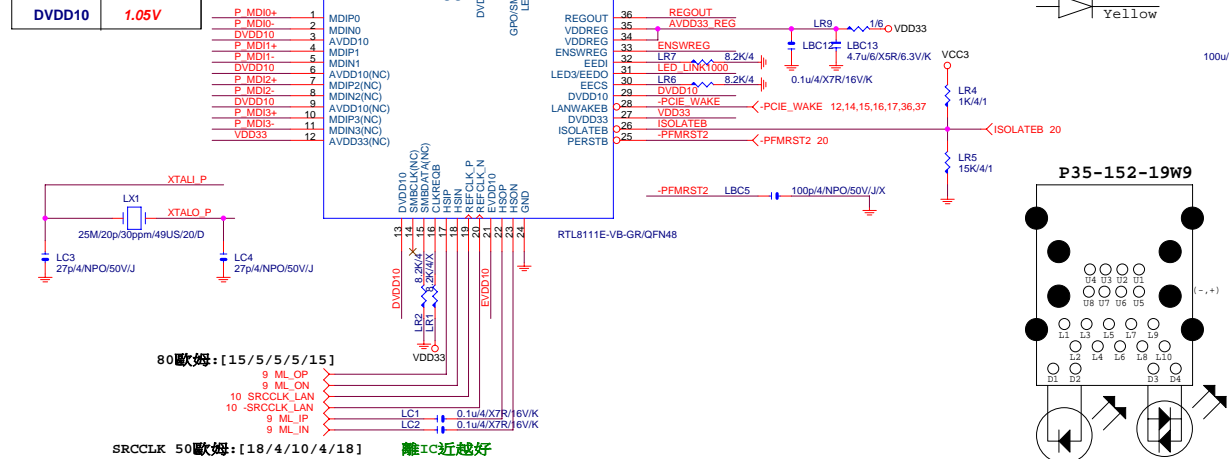
Gigabyte Technology

Title			
HWM,KB/MS, FAN CTRL			
Size	Document Number	Rev	
Custom	GA-P67A-UD3P-B3	1.1	
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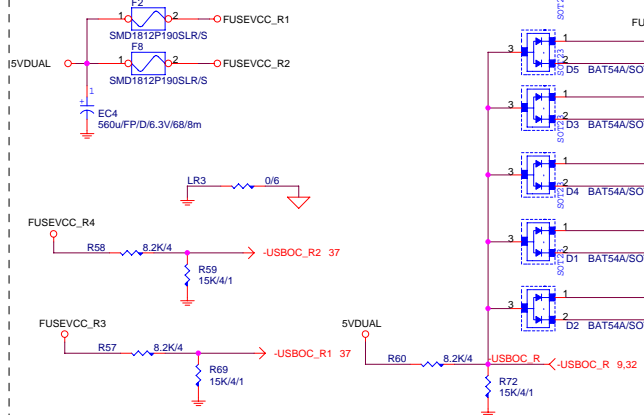
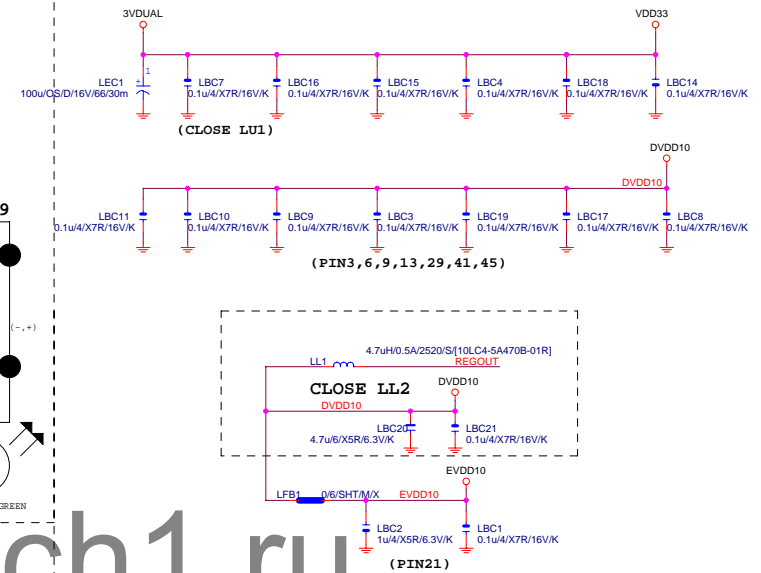
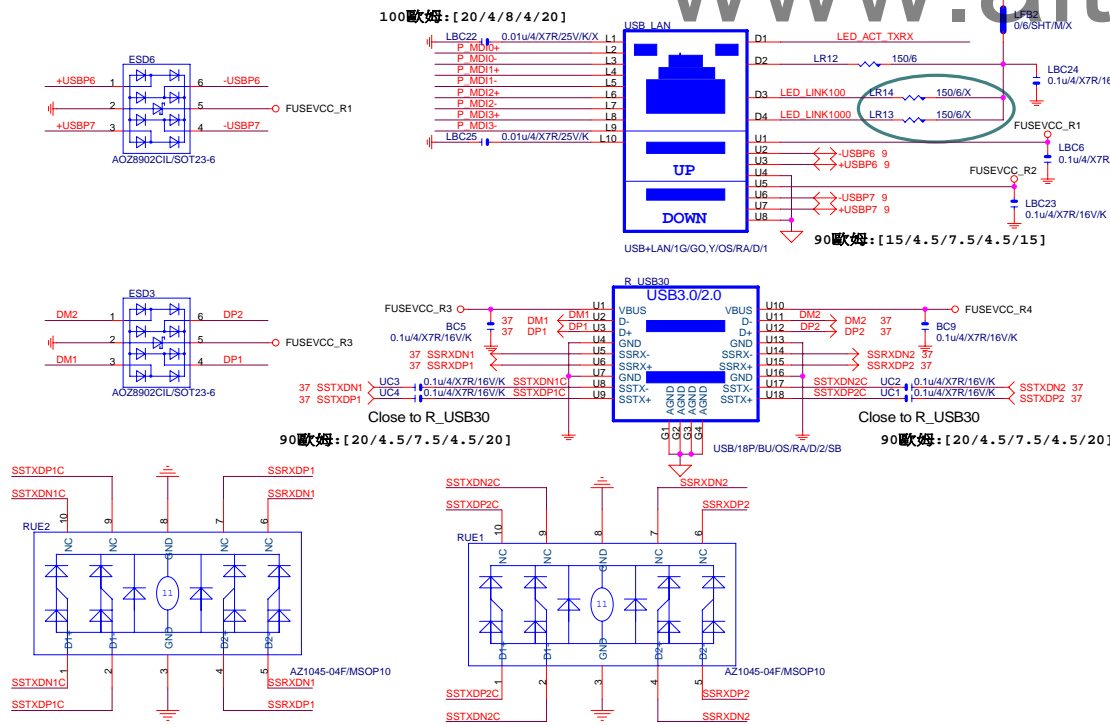
PCIE-1G LAN

Power domain chart

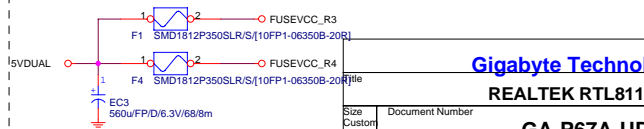
	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V



USB30_LAN CONNECTOR



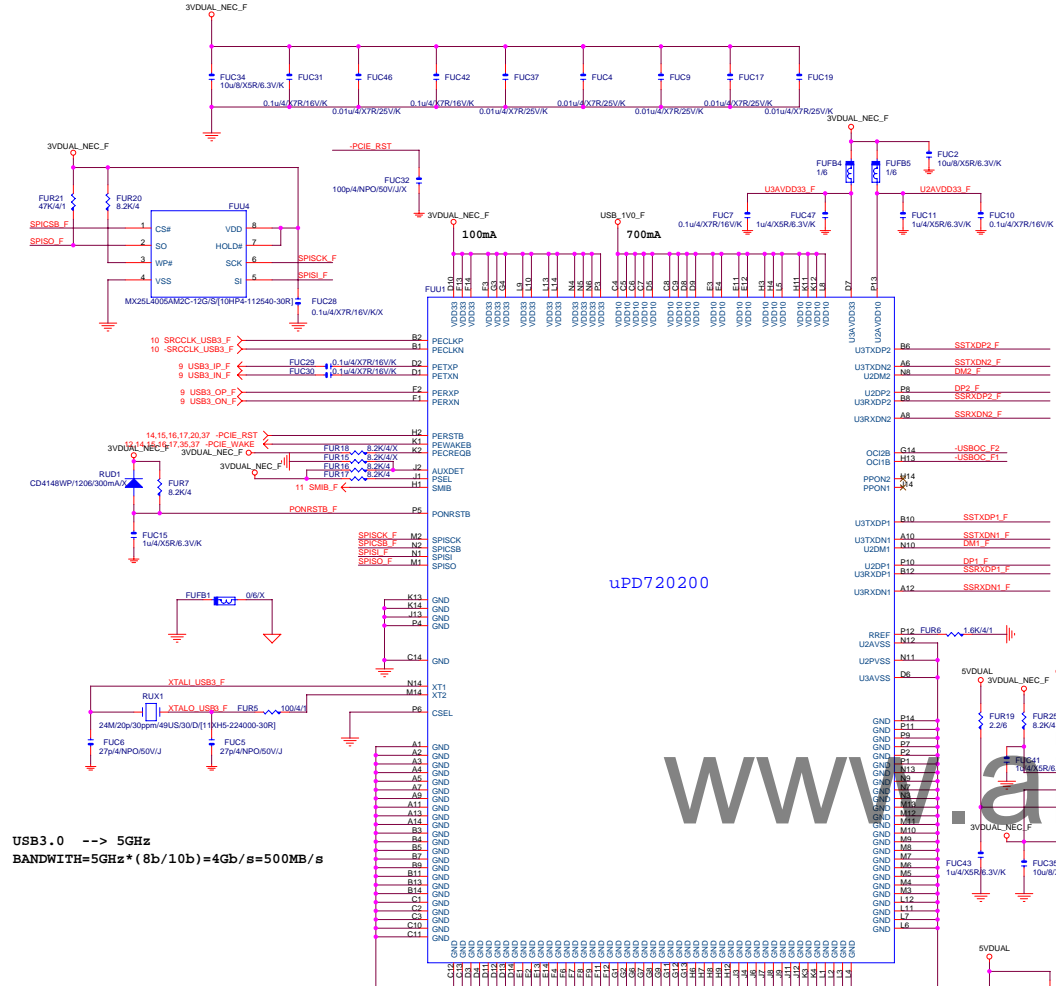
Close to connector



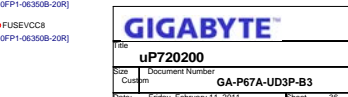
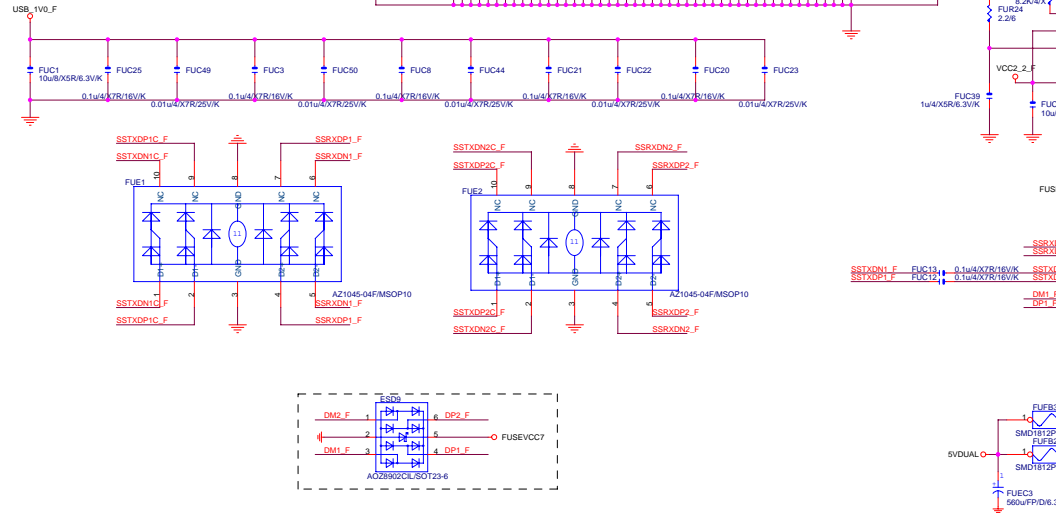
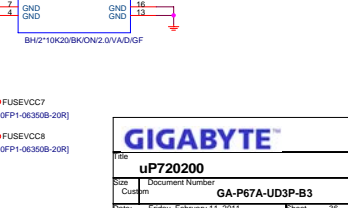
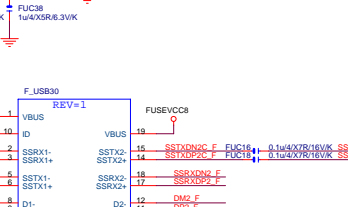
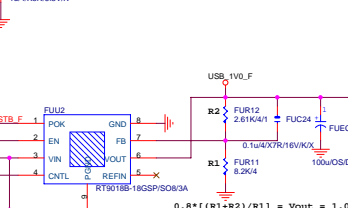
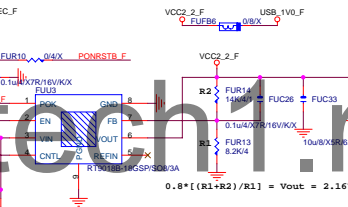
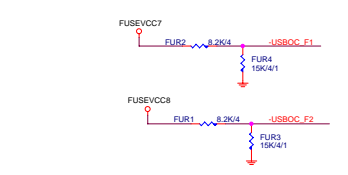
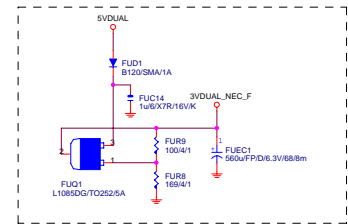
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REALTEK RTL8111D_1

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USB3.0 --> 5GHz
BANDWIDTH=5GHz*(8b/10b)=4Gb/s=500MB/s

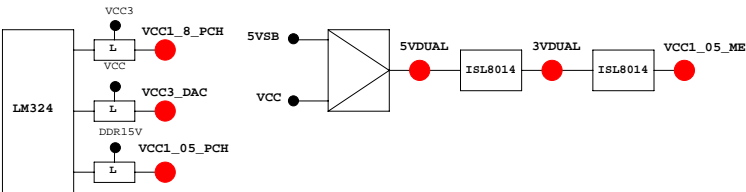


GIGABYTE		
uPD720200		
Size	Document Number	Rev
GA-P67A-UD3P-B3		1.1
Date: Friday, February 11, 2011		

PIN NAME	PWR	AFTER RESET	Default	USAGE	NOTE
GP0	MAIN	H-Z	GPI	-PECI_REQ	N/A
GP1/TACH1	MAIN		GPI	ICH_FAN_TACH1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN		GPI	ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO	GPIO8	P/U 8.2K 3VDUAL
GP9/OC5#	STBY		NATIVE	OC5#	N/A
GP10/OC6#	STBY		NATIVE	OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	-SMBALERT	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL
GP13	STBY	L	GPI	GPIO13	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	OC7#	N/A
GP15	STBY	L	GPO	GPIO15	N/A
GP16	MAIN		GPI	-SKTOCC	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	ICH_FAN_TACH0	N/A
GP18	MAIN		NATIVE	MB_ID0	P/D 8.2K GND
GP19	MAIN		GPI	-LAN1_ISO	P/U 8.2K VCC3
GP20	MAIN		NATIVE	LED_CTL	P/U 1K VCC3
GP21	MAIN		GPI	VCC18_PCH_OV2	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	VCORE_OV1	P/U 8.2K VCC3
GP23	MAIN		NATIVE	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	L	GPO	TLs	P/U 8.2K 3VDUAL
GP25	STBY		NATIVE	-CPU_STOP	P/U 8.2K 3VDUAL
GP26	STBY		NATIVE	-ACZ_DET	P/U 8.2K 3VDUAL
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	GPIO28	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	S_PWR_ACK	P/U 100K 3VDUAL
GP31	STBY	H-Z	GPI	N/A(Reverse)	P/U 8.2K VCC3
GP32	MAIN	H	GPO	MB_ID1	P/D 8.2K GND
GP33	MAIN	H	GPO	LOAD-LINE	P/U 1K VCC3
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	GPIO35	P/U 8.2K VCC3
GP36	MAIN		GPI	-LAN1_DSM	P/U 8.2K VCC3
GP37	MAIN		GPI	N/A	P/U 8.2K VCC3
GP38	MAIN	H-Z	GPI	VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	-LAN_DSM	P/U 8.2K VCC3
GP40	STBY		NATIVE	OC1#	N/A
GP41	STBY		NATIVE	OC2#	N/A
GP42	STBY		NATIVE	OC3#	N/A
GP43	STBY		NATIVE	OC4#	N/A
GP44	STBY	L	NATIVE	N/A	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	-LPCPME	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	PWR_LED	P/U 8.2K 3VDUAL
GP47	STBY		NATIVE	PSI_LED	P/U 8.2K 3VDUAL
GP48	MAIN	H-Z	IN	EN_PWM	P/U 8.2K VCC3
GP49	MAIN	H-Z	IN	VCC18_OV1	P/U 8.2K VCC3
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY		NATIVE	1_05V_OV1	P/U 8.2K 3VDUAL
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	~PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	~KBRST	
SO/GP50	~ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	~LAN2_DSM	
PSION#/GP42	~PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	~PCIE_RST	
RSMRST#CIRRX1/GP55	~RSMRST	
PME#/GP54	~LPCPME	
PD5/GP75/BUS00	N/A	

PIN	PIN NAME	USAGE	NOTE
FAN_TAC2/GP52		FANIO2	
FAN_TAC3/GP37		FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#		FANIO4	
FAN_CTL2/GP51		FANPWM2	
FAN_CTL3/GP36		FANPWM3	
VID4/GP34		BEEP-	
VID3/GP33		TURBO1	
VID2/GP32		TURBO0	
VCORE_GOOD/VID6/GP63		CPUT_LED1_C	
VID5/GP35		CPUT_LED2_C	
VID1/GP31		CPUT_LED3_C	
VID0/GP30		-LAN1_DSM	NBT_LED1_C
SLCT/GP80		CPU_LED1_C	
PE/GP81		CPU_LED2_C	
BUSY/GP82		CPU_LED3_C	
PD3/GP73/BUSS11		SB_LED1_C	
PD4/GP74/BUSS12		SB_LED2_C	
VCORE_EN/VID7/GP64		IT_GP64	SB_LED3_C
PD0/GP70		NB_LED1_C	
PD1/GP71		NB_LED2_C	
PD2/GP72/BUSS10		NB_LED3_C	
GP22/SCX		LOW_PWR_1	
VID05/GP27/SDM2		LOW_PWR_2	
PCIRST2#/GP11		-PWRST1	
PCIRST1#/GP12		-PWRST2	
3VSBSEN#/GP40		CSI_F0	BSEL166_1
SUSC#/GP53		CSI_F1	BSEL166_2
GP23/SI		BSEL166_3/CSISSBL	
VID00/GP20/CTS2#		CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01		MB_ID2	
PD6/GP76/BUSS01		MB_ID3	
PD7/GP77/BUSS02		MB_ID4	
AFD#/GP86/SMBC_R		2X PIN	FST_2X8
INIT#/GP85/SMBD_M		SEC_2x8	GT1REF_AD2
ACK#/GP83		DDR_LED1_C	
VID01/GP21/DCD2#		DDR_LED2_C	
STB#/GP87/SMBC_M		DDR_LED3_C	
PWRON#/GP44		VCORE_OV1	
PANSWH#/GP43		PWRBTSW	
KDAT/GP61		-PWRBTSW	
KCLK/GP60		KDAT	
MDAT/GP57		KCLK	
MACL/GP56		MDAT	
GP66/VLDT_EN/GB_02		NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTXX/GP15		PWM2_CR	
KDAT/GP61		PWM2_CR	
GP67/CPU_PG/GB_03		EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R		-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16		-THERM	
VID04/GP26/SOUT2		DDR18V_PH2_EN	
VID02/FAN_TAC5/GP24/DSR2#		DDR18V_LED	
VID06/GP17/RI2#		1_1V_PH_EN	
VID07/JP6/DTR2#		JP6	
PD5/GP75/BUSS00		SB_LED3_C	



The diagram illustrates a multi-processor system architecture. At the top, there are three processor blocks, each containing two cores: PH1 and PH2, PH3 and PH4, and PH5 and PH6. Below each processor block is a local cache: DL2 and DL4 for the first processor, DL9 and DL7 for the second, and DL3 and DL5 for the third. In the center is a large CPU block. To the left of the CPU is a PCH (Platform Controller Hub) block. To the right of the CPU is a VTT (Voltage Tuning Table) block, which contains two sub-blocks: one with PH1, PH2, L4, and L3; another with PH4, PH3, DL8, and DL6. Further to the right is a VCore block, which contains two sub-blocks: one with PH4 and PH3; another with DL8 and DL6. The VTT and VCore blocks are connected to the CPU block.

散熱模組料號:

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Termination
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

8IBP:
1.12SP2-01A001-Y1R/Y2R
2.12SP2-01A001-Z1R/Z2R
(HIBRID模組)包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

Gigabyte Technology			
Title			
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